FD6636S

600V 3-PHASE BRIDGE DRIVER

Description

The FD6636S is an integrated 3-phase half-bridge gate driver IC designed for high voltage, high speed power MOSFETs and IGBTs that operate up to +600V.

The FD6636S has also built-in cross-conduction and deadtime prevention logic. It can also prevent the short-circuit turning on of MOSFETs and IGBTs, thus protect effectively the power devices.

The FD6636S has also built-in VCC and VB undervoltage(UVLO) protection to prevent the power semiconductor devices from operation under very low voltage.

The FD6636S has built-in input signal filtering to prevent input noise.

The FD6636S has built-in over-current function is available to turn off all six drivers.

The FD6636S has also built-in enable function is available to terminate all six outputs.

Features

- Suspension absolute voltage +600V
- Independent 3 half-bridge drivers
- Output current: +0.21A/-0.36A
- 3.5V/5V input logic compatible
- VCC/VBS Undervoltage protection (UVLO)
- High and low channel matching
- Output is out of phase with the input
- Cross-conduction prevention logic
- Built-in dead time
- Enable function
- Built-in input noise filter
- Over-current shutdown turn off all six drivers
- Externally programmable delay for automatic fault clear
- RoHS compliant

Packages

SOP28

Applications

- Motor drives
- DC-AC inverter drives

1. Absolute Maximum Rating (All pins are referenced to COM unless otherwise stated)

Parameter	Symbol	Min~Max	Units
High side floating absolute voltage	$V_{B1,2,3}$	-0.3～625	V
High side floating offset	$V_{S1,2,3}$	$V_{B1,2,3}$-25～$V_{B1,2,3}$+0.3	V
High side output voltage	$V_{HO1,2,3}$	$V_{S1,2,3}$ -0.3～$V_{B1,2,3}$ +0.3	V
Low side supply voltage	V_{CC}	-0.3～25	V
Logic ground	V_{SS}	V_{CC} -25～V_{CC}+0.3	V
Low side output voltage	$V_{LO1,2,3}$	-0.3～V_{CC}+0.3	V
Logic input voltage（HIN*,LIN*,ITRIP,EN）	V_{IN}	V_{SS}-0.3～V_{CC}+0.3	V
RCIN input voltage	V_{RCIN}	V_{SS}-0.3～V_{CC}+0.3	V
FAULT* input voltage	V_{FLT}	V_{SS}-0.3～V_{CC}+0.3	V
Offset voltage slew rate range	dV_S/dt	≤50	V/ns
Power dissipation @T_A≤25°C	P_D	≤1.8	W
Thermal resistance, junction to ambient	R_{thJA}	≤70	°C/W
Junction temperature	T_j	≤150	°C
Storage temperature	T_{stg}	-55～150	°C

Note1: In any case, power dissipation should not exceed P_D.

Note2: Voltages above the absolute maximum ratings may damage the chip.

2. Recommended Operating Conditions (All voltages are referenced to COM)

Definition	Symbol	Min	Max	Units
High-side float absolute voltage	$V_{B1,2,3}$	$V_{S1,2,3}$+10	$V_{S1,2,3}$+20	V
High-side floating offset voltage	$V_{S1,2,3}$	Note1	600	V
High-side output voltage	$V_{HO1,2,3}$	$V_{S1,2,3}$	$V_{B1,2,3}$	V
Low-side supply voltage	V_{CC}	10	20	V
Low side output voltage	$V_{LO1,2,3}$	0	V_{CC}	V
Logic ground	V_{SS}	-5	5	V
FAULT* input voltage	V_{FLT}	V_{SS}	V_{CC}	V
RCIN input voltage	V_{RCIN}	V_{SS}	V_{CC}	V
ITRIP input voltage	V_{ITRIP}	V_{SS}	V_{CC}	V
Logic input voltage（HIN*, LIN*,EN）	V_{IN}	V_{SS}	V_{CC}	V
Environment temperature	T_A	-40	125	°C

Note1: Logic operational for V_S of (COM – 5V) to (COM + 600V). Logic state held for V_S of (COM – 5V) to (COM –V_{BS}).

Note2: The long-term operation of the chip outside the recommended conditions may affect its reliability. It is not recommended to work in an environment that exceeds the recommended conditions.

3. Electrical Characteristics (T_A =25°C，V_{CC}=$V_{BS1,2,3}$=15V，C_L=1000pF，$V_{S1,2,3}$= V_{SS}=COM, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent V_{CC} supply current	I_{QCC}	V_{IN} =0V or 5V	--	0.9	1.6	mA
Quiescent V_{BS} supply current	I_{QBS}	V_{IN}=0V or 5V	--	90	150	μA
Offset supply leakage current	I_{LK}	$V_{B1,2,3}$=$V_{S1,2,3}$=600V	--	0.1	5.0	μA
Logic “1” input voltage	V_{IH}		2.7	--	--	V
Logic “0” input voltage	V_{IL}		--	--	0.8	V
Enable positive going threshold	$V_{EN,TH+}$		--	--	2.7	V
Enable negative going threshold	$V_{EN,TH-}$		0.8	--	--	V
ITRIP positive going threshold	$V_{IT,TH+}$		0.38	0.46	0.54	V
ITRIP input hysteresis	$V_{IT,HYS}$		--	0.08	--	V
RCIN positive going threshold	$V_{RCIN,TH+}$		--	8	--	V
RCIN input hysteresis	$V_{RCIN,HYS+}$		--	3	--	V
Input bias current(LOUT=LOW)	I_{LIN*+}	V_{LIN*}=5V	--	70	100	μA
Input bias current(LOUT=HIGH)	I_{LIN*-}	V_{LIN*}=0V	--	110	150	μA
Input bias current(HOUT=LOW)	I_{HIN*+}	V_{HIN*}=5V	--	70	100	μA
Input bias current(HOUT=HIGH)	I_{HIN*-}	V_{HIN*}=0V	--	110	150	μA
Logic “1” ITRIP input bias current	I_{ITRIP+}	V_{ITRIP}=5V	--	300	500	μA
Logic “0” ITRIP input bias current	I_{ITRIP-}	V_{ITRIP}=0V	--	0	1	μA
Logic “1” EN input bias current	I_{EN+}	V_{EN}=5V	--	300	500	μA
Logic “0” EN input bias current	I_{EN-}	V_{EN}=0V	--	0	1	μA
RCIN input bias current	I_{RCIN}	V_{RCIN}=0V or 15V	--	0	1	μA
V_{CC} supply undervoltage positive going threshold	V_{CCUV+}		8.1	9.0	9.9	V
V_{CC} supply undervoltage negative going threshold	V_{CCUV-}		7.5	8.4	9.3	V
V_{CC} supply undervoltage lockout hysteresis	V_{CCUVH}		0.4	0.6	--	V
V_{BS} supply undervoltage positive going threshold	V_{BSUV+}		8.0	8.9	9.8	V
V_{BS} supply undervoltage negative going threshold	V_{BSUV-}		7.3	8.1	8.9	V
V_{BS} supply undervoltage lockout hysteresis	V_{BSUVH}		0.5	0.8	--	V
High level output voltage, V_{BIAS} - V_O	V_{OH}	I_O=20mA	--	0.6	1.0	V
low level output voltage, V_O	V_{OL}	I_O=20mA	--	0.2	0.35	V
Output high short circuit pulsed current	I_{OH}	V_O=0V，V_{IN}=0V，PWD≤10μs	0.14	0.21	--	A
Output low short circuit pulsed current	I_{OL}	V_O=15V，V_{IN}=5V，PWD≤10μs	0.24	0.36	--	A
RCIN low on resistance	R_{ON_RCIN}		--	50	75	Ω

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
FAULT* low on resistance	R_{ON_FAULT*}		--	50	75	Ω
Output rising edge transmission time	t_{on}	C_L=1000pF	200	300	400	ns
Output falling edge transmission time	t_{off}	C_L=1000pF	200	300	400	ns
Output rising time	t_r	C_L=1000pF	--	110	180	ns
Output falling time	t_f	C_L=1000pF	--	45	70	ns
ENABLE low to output shutdown propagation delay	t_{EN}	V_{EN} =0V	200	300	400	ns
ITRIP to output shutdown propagation delay	t_{ITRIP}	V_{ITRIP}=5V	275	400	525	ns
ITRIP blanking time	t_{bl}	V_{IN}=0V,V_{ITRIP}=5V	100	150	--	ns
ITRIP to FAULT* Propagation delay	t_{FLT}	V_{IN}=0V,V_{ITRIP}=5V	200	325	450	ns
Input filter time(HIN*,LIN*)	t_{FILIN*}	V_{IN}=0V	100	200	--	ns
FAULT clear time RCIN: R=2M,C=1nF	t_{FLTCLR}	V_{IN}=0V,V_{ITRIP}=0V	1.3	1.65	2.0	ms
Deadtime	DT	V_{IN}=0V or 5V	200	300	400	ns
High-low side delay match	MT	External deadtime>400ns	--	40	75	ns
Matching delay,max(t_{on}, t_{off})-min(t_{on}, t_{off})	MDT		--	25	70	ns
Output pulse width matching	PM	|pwin-pwout|	--	40	75	ns

Note：For high side PWM, HIN1,2,3* pulse width must be≥1μs

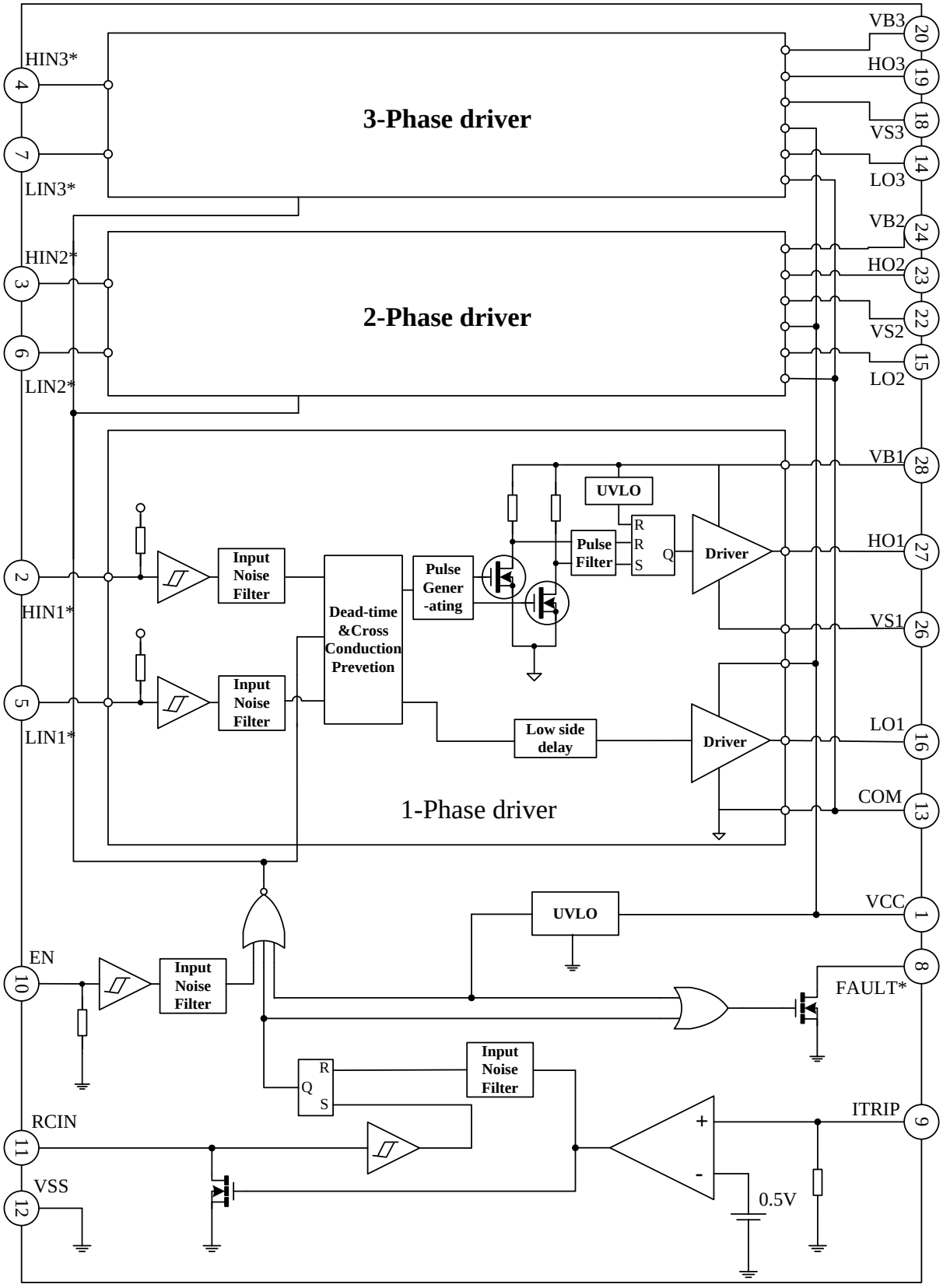
V_{CC}	V_{BS}	ITRIP	EN	FAULT	LO	HO
<V_{CCUV-}	X	X	X	0（Note1）	0	0
15V	<V_{BSUV-}	0V	5V	High imp	LIN1,2,3	0
15V	15V	0V	5V	High imp	LIN1,2,3	HIN1,2,3
15V	15V	>$V_{IT,TH+}$	5V	0（Note 2）	0	0
15V	15V	0V	0V	High imp	0	0

Note1：·V_{CCUV-} is not latched，when V_{CC}> V_{CCUV-}，FAULT returns to high impedance.

Note2：·When ITRIP< $V_{IT,TH-}$，FAULT returns to high impedance after RCIN pin becomes greater than 8V (@VCC=15V).

Note3：·A Cross-conduction prevention logic prevents LO1,2,3 and HO1,2,3 for each channel from turning-on simultaneously.

4. Circuit diagram



5. Chip pin configuration

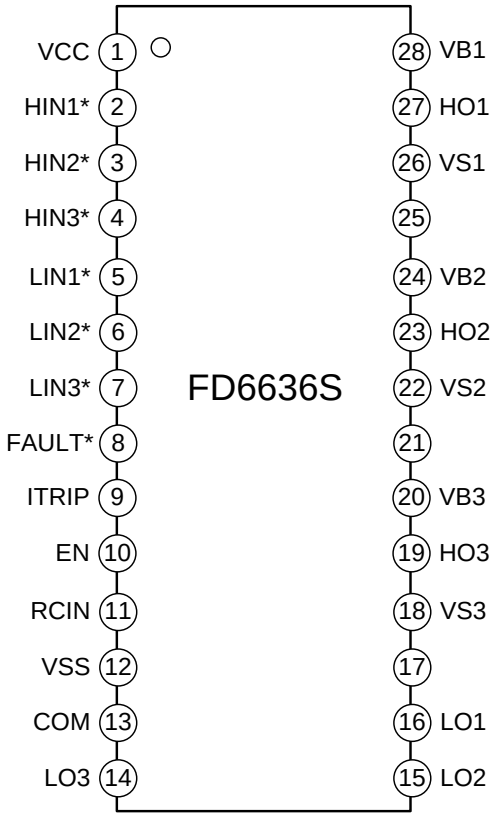
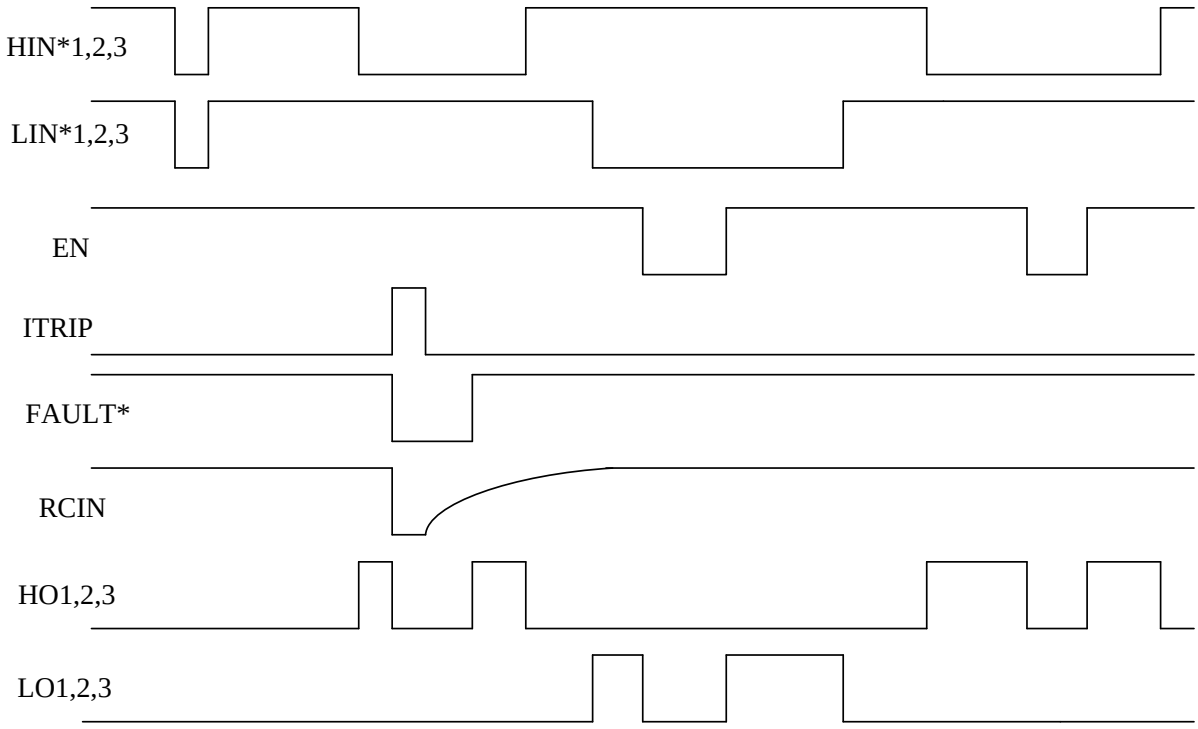


Figure 5-1 Package pin diagram

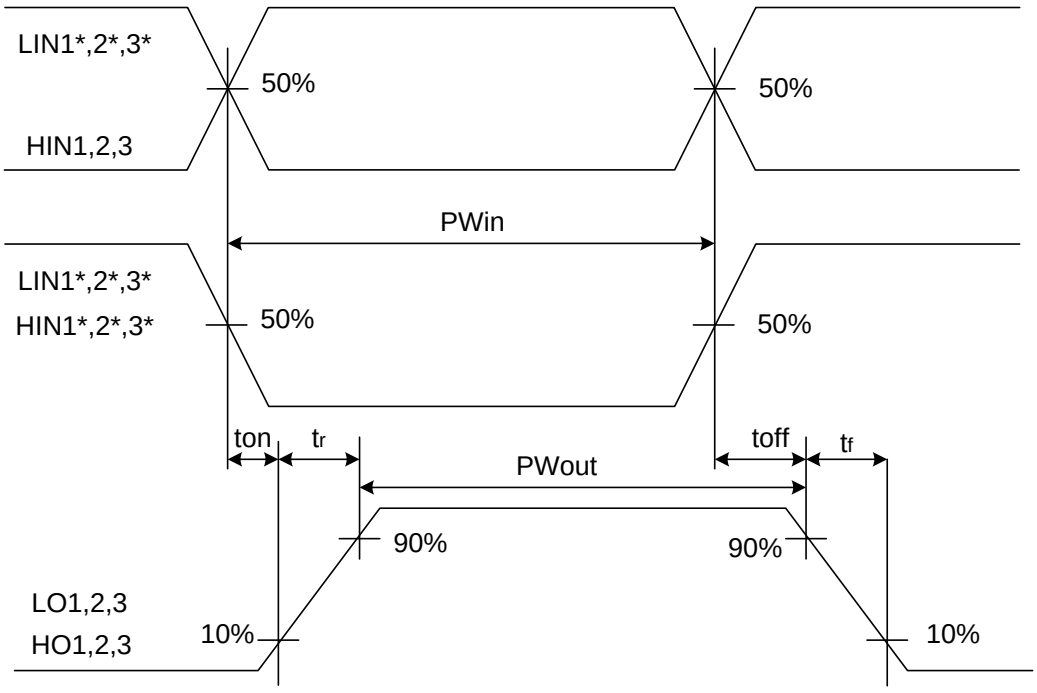
Table 5-1 Package pin

Pin no.	Pin name	Pin description
1	VCC	Low-side supply voltage
2,3,4	HIN1*,HIN2*,HIN3*	High-side input, out of phase
5,6,7	LIN1*,LIN2*,LIN3*	Low-side input, out of phase
8	FAULT*	Indicates over-current (ITRTIP) or low-side undervoltage lockout has occurred.
9	ITRIP	Analog input for over-current shutdown.
10	EN	Logic input to enable I/O functionality.
11	RCIN	External RC network input used to define FAULT clear delay.
12	VSS	Logic ground
13	COM	Low side gate drivers return
14,15,16	LO3,LO2,LO1	Low-side output
18,22,26	VS3,VS2,VS1	High-side floating offset voltage
19,23,27	HO3,HO2,HO1	High-side output
20,24,28	VB3,VB2,VB1	High-side float absolute voltage
17,21,25	NC	Not Connected

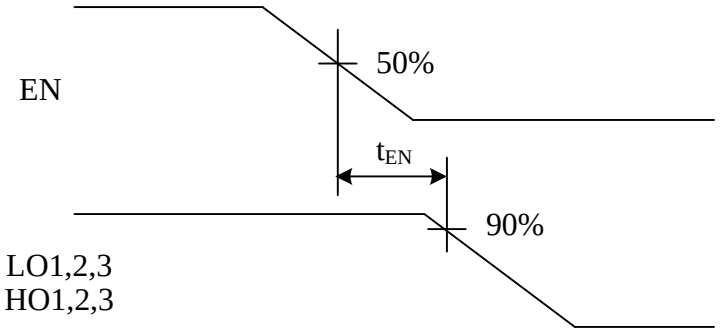
6. Logic timing diagram



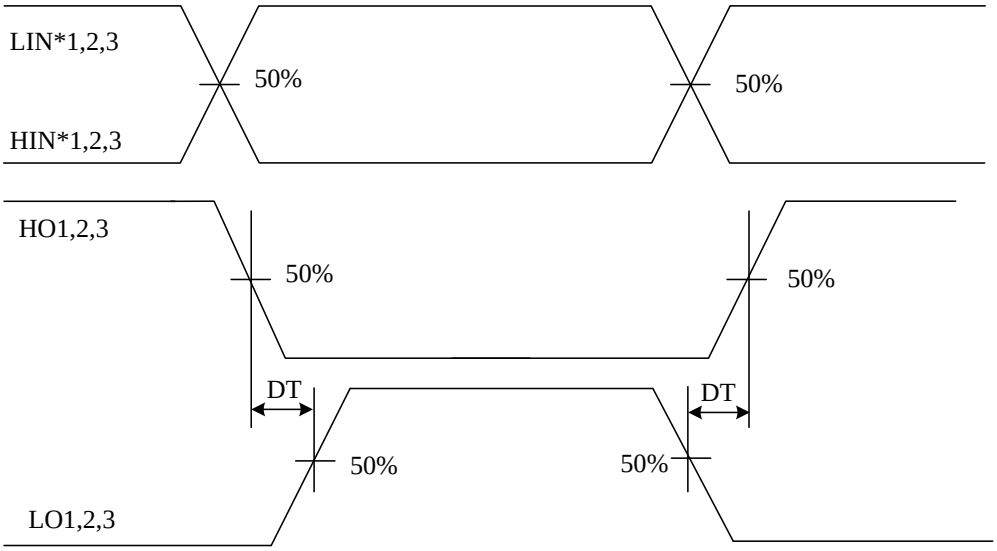
7. Switching time test standards



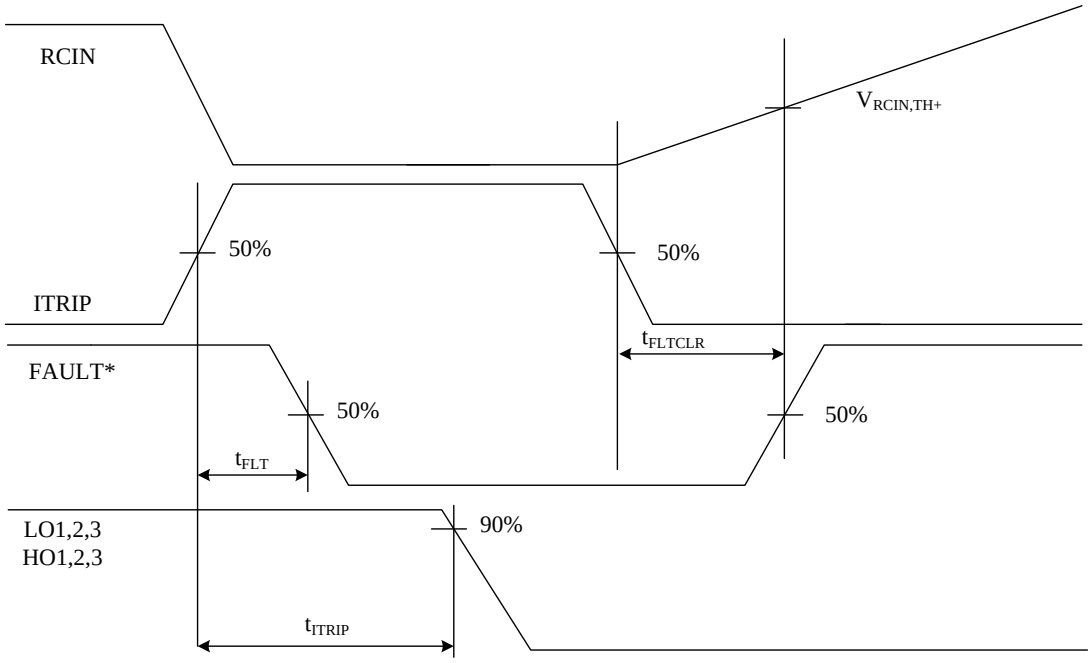
8. Enable time test standards



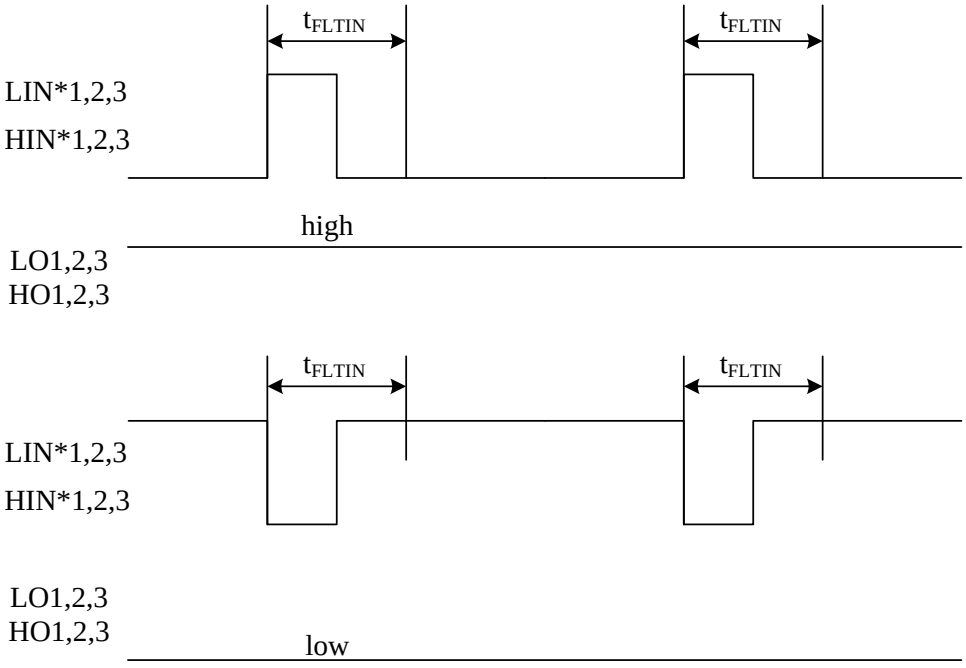
9. Dead time test standards



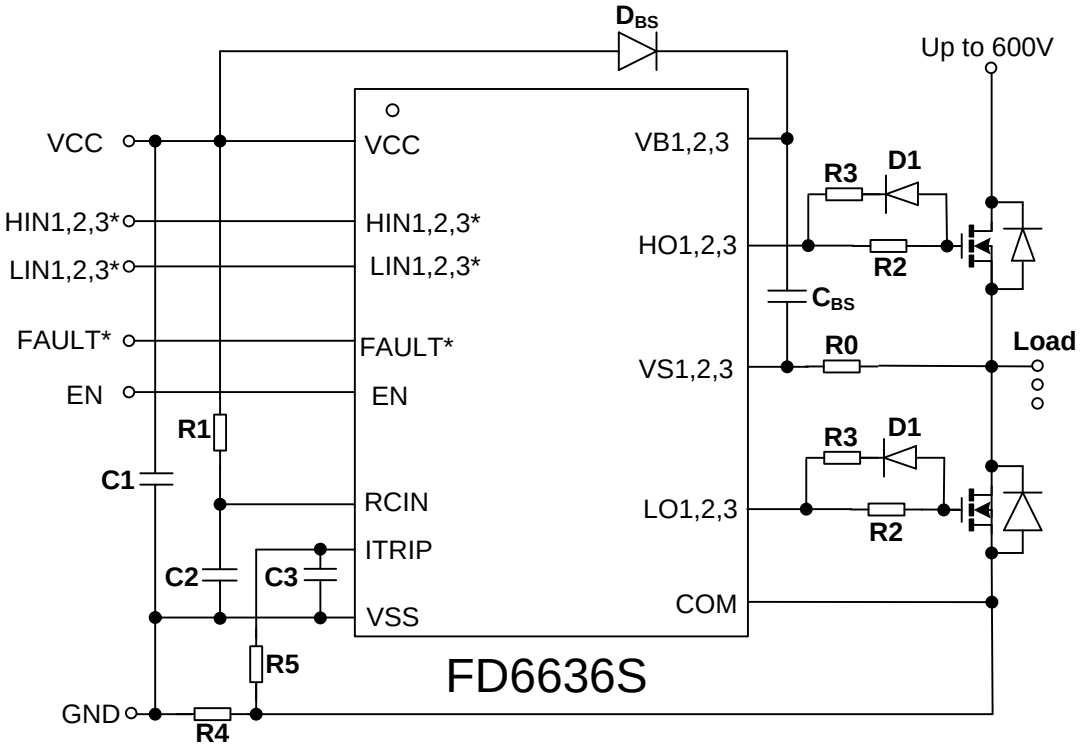
10. ITRIP/RCIN time test standards



11. Input Filter Function



12. Typical application circuit



C1： Power filter capacitor, according to the circuit can choose 1μF ~ 10μF, as close to the chip pin as possible.

C2： according to the circuit can choose 1nF.

C3： according to the circuit can choose 10nF.

R0： according to the circuit can choose 1Ω~6Ω.

R1： according to the circuit can choose 2MΩ.

R2/R3：Gate drive resistor, and the resistance depends on the device being driven.

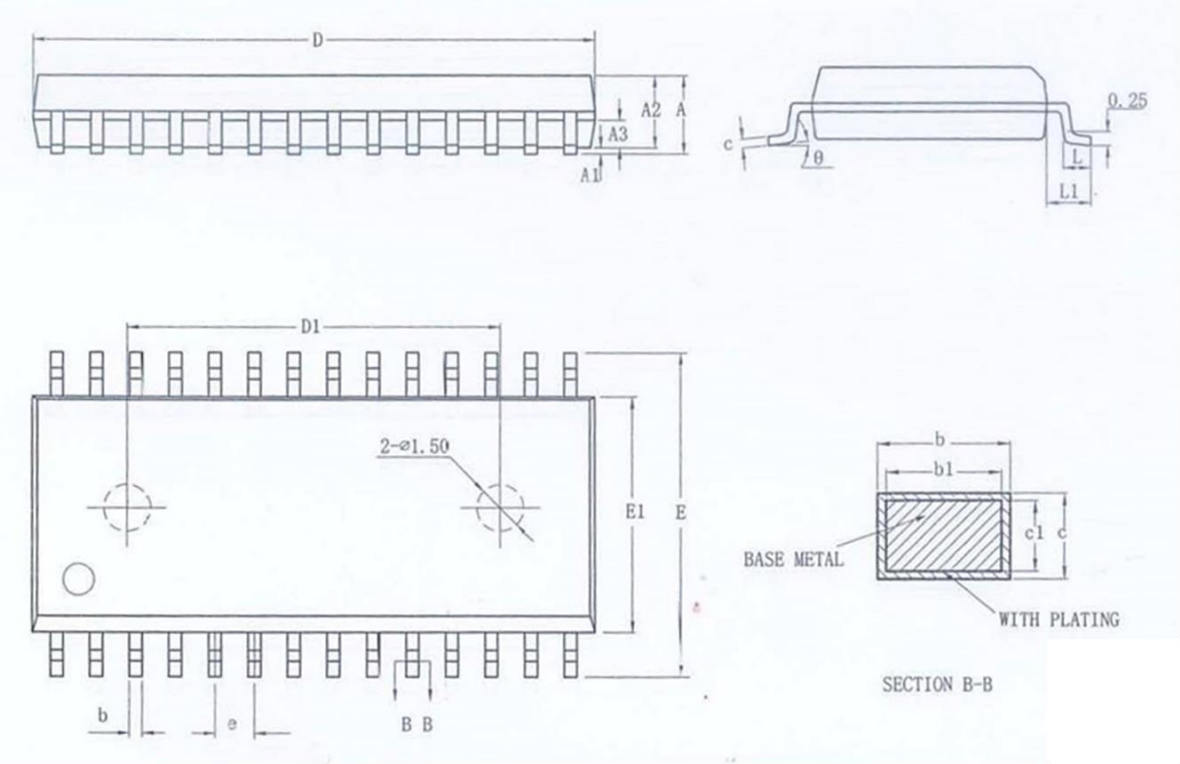
Dbs：Bootstrap diodes. It should be selected for high reverse breakdown voltage Schottky diodes.

Cbs：Bootstrap capacitors. Ceramic capacitors or tantalum capacitors should be selected, according to the circuit can choose 0.22μF ~ 10μF. The capacitor should be as close as possible to the chip pin.

Note:

The above circuits and parameters are for reference only. The actual application circuit should be designed with the measured results with setting the parameters.

13. Package size（SOP28）



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	2.65
A1	0.10	—	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.39	—	0.48
b1	0.38	0.41	0.43
c	0.25	—	0.31
c 1	0.24	0.25	0.26
D	17.80	18.00	18.20
D1	11.90	12.00	12.10
E	10.10	10.30	10.50
E1	7.30	7.50	7.70
e	1.27BSC		
L	0.70	—	1.00
L1	1.40BSC		
θ	0	—	8^0

Product number	Package	Marking	Packing	Quantity
FD6636S	SOP28	FD6636S	Tape & Reel	1000

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