

# FD2103P

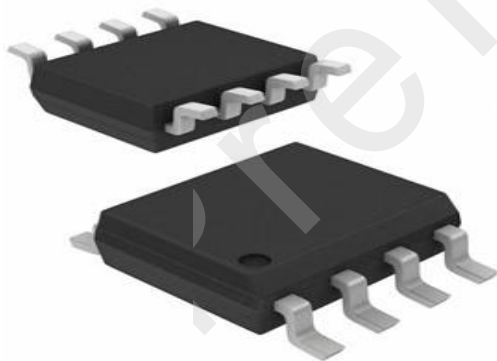
## Overview

FD2103P is a Half-bridge Gate Driver designed for driving high-voltage, high-speed N-type power MOSFET, and workable at 180V circuit.

FD2103P has built-in under-voltage (UVLO) protection to prevent the power tube at low voltage to work, and also for improving efficiency.

FD2103P has also built-in input signal filtering to prevent input noise. It can also prevent the short-circuit turning on of MOSFETs, and thus protect effectively the power devices

## Package



## 180V Half-bridge Gate Driver

## Features

- Suspension absolute voltage : +180V
- Gate driver supply range from 10V to 20V
- Output current: +0.3A/-0.6A
- Input logic compatible: 3.3V/5V
- VCC Undervoltage protection (UVLO)
- Output of high side is in phase with the input of high side
- Output of low side is phase reversal with the input of low side
- Cross-conduction prevention
- Built-in 100ns dead time zone

## Application

Motor drive

DC-DC converter

## 1. Absolute maximum rating (Unless otherwise noted, all pins refer to COM as a reference point)

Parameter	Symbol	Range	Unit
High-side float absolute voltage	$V_B$	-0.3~205	V
High-side floating offset voltage	$V_S$	$V_B-25\sim V_B+0.3$	V
High-side output voltage	$V_{HO}$	$V_S-0.3\sim V_B+0.3$	V
Low-side supply voltage	$V_{CC}$	-0.3~25	V
Low side output voltage	$V_{LO}$	-0.3~ $V_{CC}+0.3$	V
Logic input voltage (HIN, LIN*)	$V_{IN}$	-0.3~6.5	V
Offset voltage slew rate range	$dV_S/dt$	$\leq 50$	V/ns
Power dissipation @ $T_A\leq 25^\circ\text{C}$	SOIC-8 $P_D$	$\leq 0.625$	W
Thermal resistance, junction to the ambient	SOIC-8 $R_{thJA}$	$\leq 200$	$^\circ\text{C/W}$
Junction temperature range	$T_j$	$\leq 150$	$^\circ\text{C}$
Storage temperature range	$T_{stg}$	-55~150	$^\circ\text{C}$

### Note:

- 1: Do not exceed  $P_D$  under any circumstances
- 2: Voltage exceeding absolute maximum ratings may damage the chip.

## 2. Recommended working conditions (All voltages are referenced to COM)

Parameter	Symbol	Min	Mnx	Unit
High-side float absolute voltage	$V_B$	$V_S+10$	$V_S+20$	V
High-side floating offset voltage	$V_S$	-5	180	V
High-side output voltage	$V_{HO}$	$V_S$	$V_B$	V
Low-side supply voltage	$V_{CC}$	10	20	V
Low side output voltage	$V_{LO}$	0	$V_{CC}$	V
Logic input voltage (HIN, LIN*)	$V_{IN}$	0	5.5	V
Environment temperature	$T_A$	-40	125	$^\circ\text{C}$

### Note:

1. The reliability of the chip could be affected if it operates with long-term in the recommended working conditions.

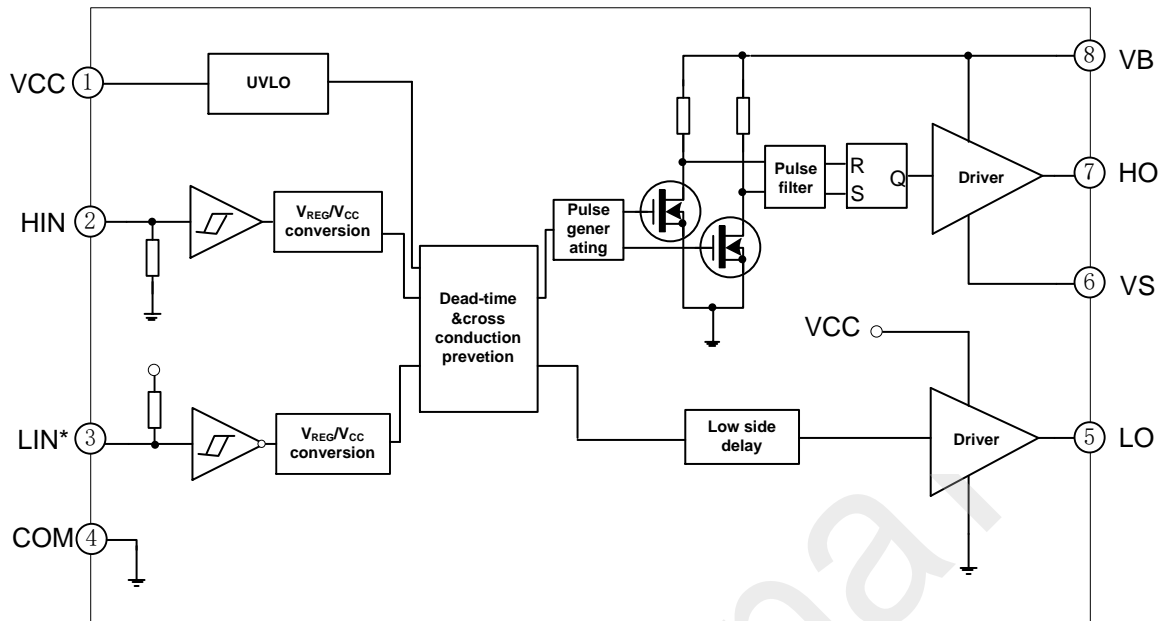
### 3. Static electrical parameters (TA =25°C, VCC=VBS=15V, VS=COM, Unless otherwise specified,)

Parameter	Symbol	Conditions	Min	Typical	Max	Unit
High level threshold input voltage	V <sub>IH</sub>		2.7	--	--	V
Low level threshold input voltage	V <sub>IL</sub>		--	--	0.8	V
V <sub>CC</sub> undervoltage protection trip voltage	V <sub>CCUV+</sub>		8.1	9.0	9.9	V
V <sub>CC</sub> undervoltage protection reset voltage	V <sub>CCUV-</sub>		7.4	8.3	9.2	V
V <sub>CC</sub> Undervoltage protection hysteresis voltage	V <sub>CCUVH</sub>		0.5	0.7	--	V
leakage current of suspended power	I <sub>LK</sub>	V <sub>B</sub> =V <sub>S</sub> =180V	--	0.1	5.0	μA
V <sub>BS</sub> Static current	I <sub>QBS</sub>	V <sub>IN</sub> =0V 或 5V	--	--	100	μA
V <sub>CC</sub> Static current	I <sub>QCC</sub>	V <sub>IN</sub> =0V 或 5V	--	450	800	uA
LIN* High-level input bias current	I <sub>LIN+</sub>	V <sub>LIN+</sub> =0V	--	60	120	μA
LIN* Low-level input bias current	I <sub>LIN-</sub>	V <sub>LIN+</sub> =5V	--	--	5	μA
HIN High-level input bias current	I <sub>HIN+</sub>	V <sub>HIN</sub> =5V	--	60	120	μA
HIN Low-level input bias current	I <sub>HIN-</sub>	V <sub>HIN</sub> =0V	--	--	5	μA
High-level output voltage	V <sub>OH</sub>	I <sub>o</sub> =20mA	--	0.5	0.85	V
Low-level output voltage	V <sub>OL</sub>	I <sub>o</sub> =20mA	--	0.12	0.2	V
High-level output short-circuit pulse current	I <sub>OH</sub>	V <sub>O</sub> =0V, PWD≤10μs	0.2	0.3	--	A
Low-level output short-circuit pulse current	I <sub>OL</sub>	V <sub>O</sub> =15V, PWD≤10μs	0.3	0.6	--	A
V <sub>S</sub> Static negative voltage	V <sub>SN</sub>		--	-7	--	V

### 4. Transient electrical parameters (TA =25°C, VCC=VBS=15V, CL=1000pFVS=COM, unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typical	Max	Unit
Output rising edge transmission time	t <sub>on</sub>	C <sub>L</sub> =1000pF	--	150	270	ns
Output falling edge transmission time	t <sub>off</sub>	C <sub>L</sub> =1000pF	--	50	100	ns
Output rising time	t <sub>r</sub>	C <sub>L</sub> =1000pF	--	70	--	ns
Output falling time	t <sub>f</sub>	C <sub>L</sub> =1000pF	--	35	--	ns
Dead-time	DT		--	100	200	ns
High-low side delay match	MT		--	--	50	ns

## 5. Circuit diagram



## 6. Chip pin configuration

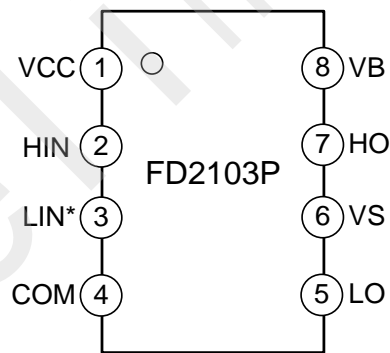
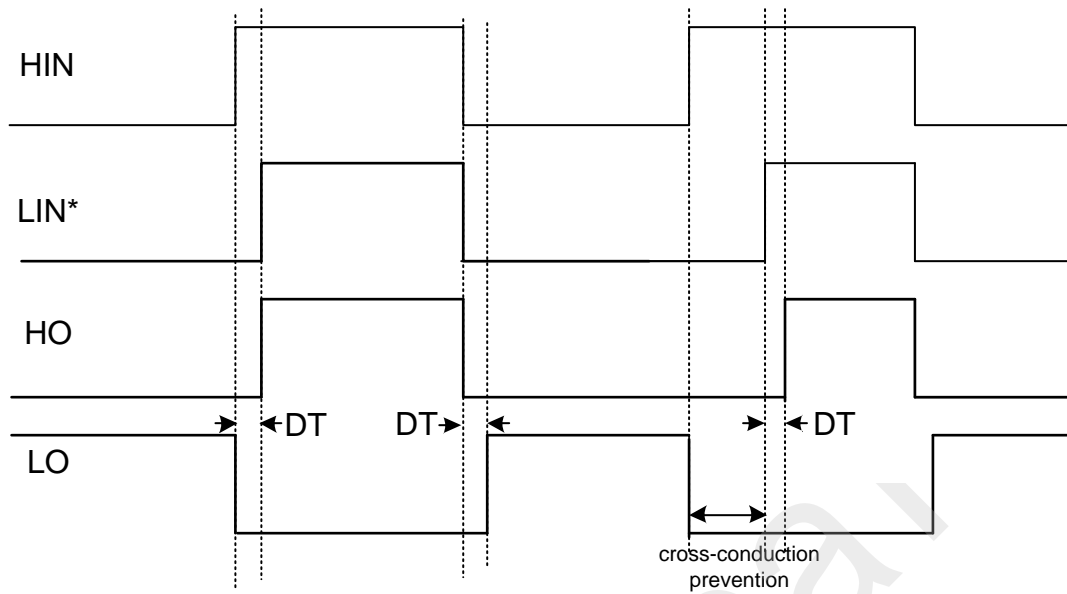


Figure 6-1 Package pin diagram

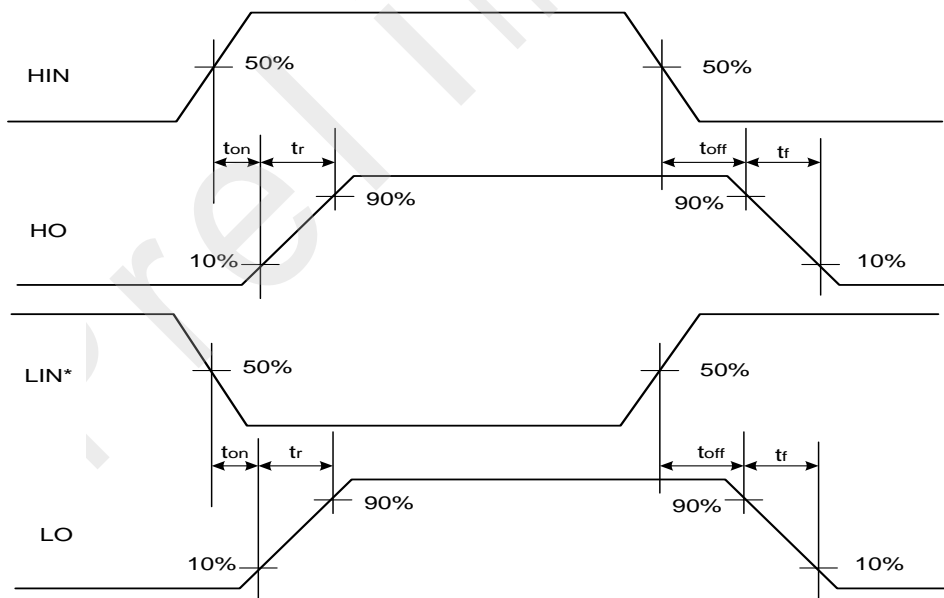
Table 6-1 Package pin

Pin no.	Pin name	Pin description
1	V <sub>CC</sub>	Low-side supply voltage
2	HIN	High-side input
3	LIN*	Low-side input
4	COM	Ground
5	LO	Low-side output
6	VS	High-side floating offset voltage
7	HO	High-side output
8	VB	High-side float absolute voltage

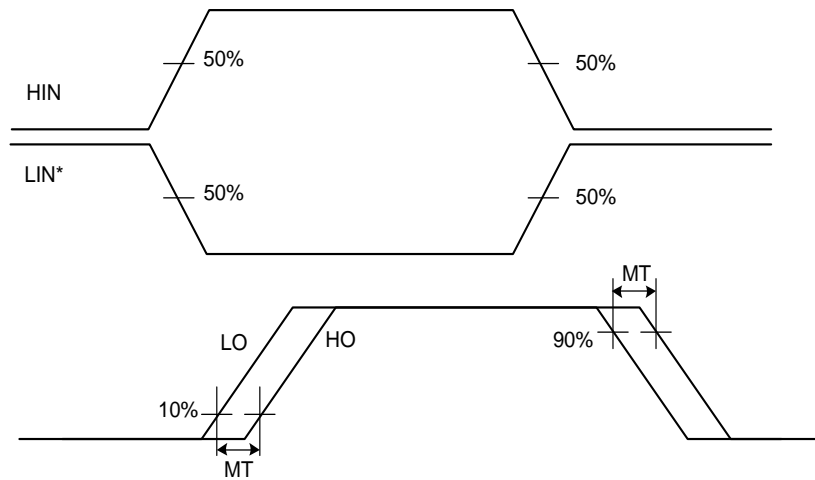
### 7. Logic timing diagram



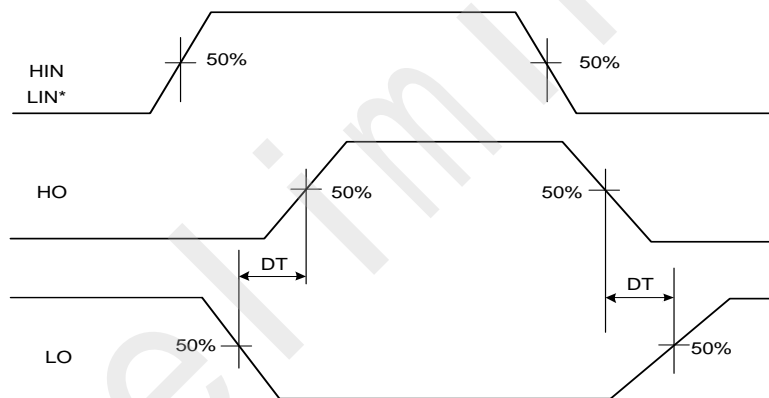
### 8. Switching time test standards



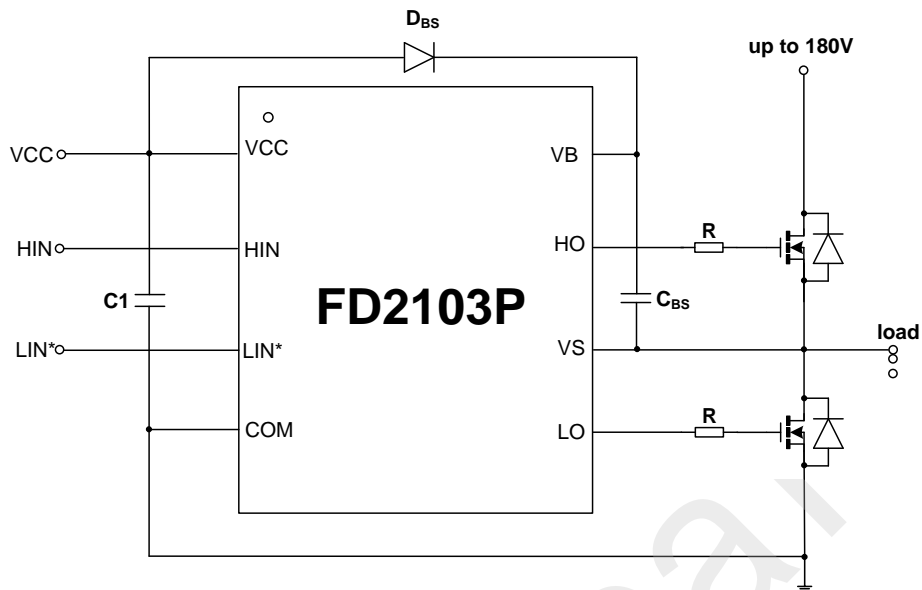
### 9. Transmission time matching test standards



### 10. Dead time test standards



## 11. Typical application circuit



**C1:** Power filter capacitor, according to the circuit can choose  $1 \mu\text{F} \sim 100 \mu\text{F}$ , as close to the chip pin as possible.

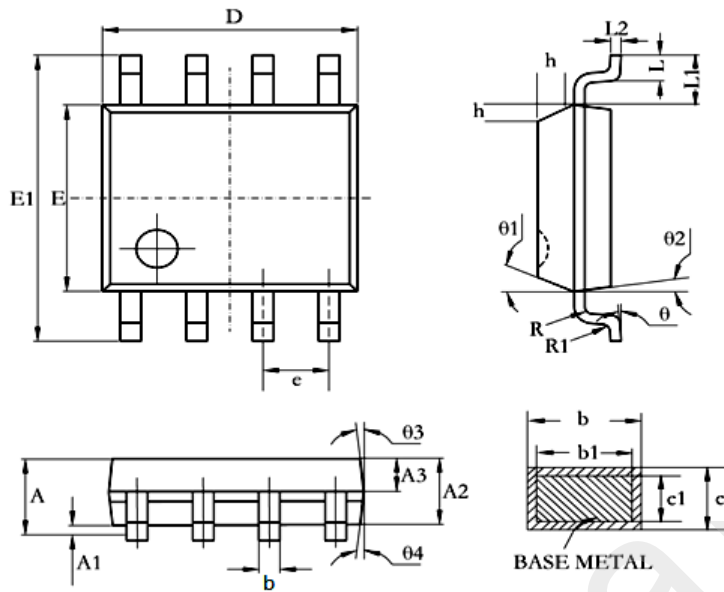
**R:** Gate drive resistor, and the resistance depends on the device being driven.

**DBS:** Bootstrap diodes. It should be selected for high reverse breakdown voltage Schottky diodes.

**Cbs:** Bootstrap capacitors. Ceramic capacitors or tantalum capacitors should be selected, according to the circuit can choose  $1 \mu\text{F} \sim 50 \mu\text{F}$ . The capacitor should be as close as possible to the chip pin.

### Note:

The above circuits and parameters are for reference only. The actual application circuit should be designed with the measured results in setting the parameters.

**12. Package size (SOIC-8)**


Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min	Nom	Max	Min	Nom	Max
A	1.36	1.55	1.75	0.053	0.061	0.069
A1	0.10	0.15	0.25	0.004	0.006	0.010
A2	1.25	1.40	1.65	0.049	0.055	0.065
A3	0.50	0.60	0.70	0.020	0.024	0.028
b	0.38	-	0.51	0.015	-	0.020
b1	0.37	0.42	0.47	0.015	0.017	0.019
c	0.17	-	0.25	0.007	-	0.010
c1	0.17	0.20	0.23	0.007	0.008	0.009
D	4.80	4.90	5.00	0.189	0.193	0.197
E1	5.80	6.00	6.20	0.228	0.236	0.244
E	3.80	3.90	4.00	0.150	0.154	0.157
e	1.27BSC					
L	0.45	0.60	0.80	0.018	0.024	0.031
L1	1.04REF					
L2	0.25BSC					
R	0.07	-	-	0.003	-	-
R1	0.07	-	-	0.003	-	-
h	0.30	0.40	0.50	0.012	0.016	0.020
θ	0°	-	8°	0°	-	8°
θ1	15°	17°	19°	15°	17°	19°
θ2	11°	13°	15°	11°	13°	15°
θ3	15°	17°	19°	15°	17°	19°
θ4	11°	13°	15°	11°	13°	15°

Part Number	Package Type	Marking	Package Method	Quantity
FD2103P	SOIC-8	FD2103P	Tape&Reel	3000



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