

# FD2203S

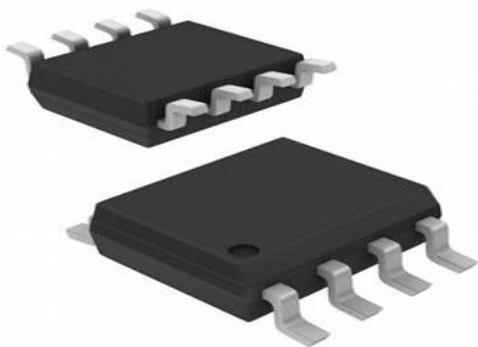
## Overview

FD2203S is a Half-bridge Gate Driver designed for driving high-voltage, high-speed N-type power MOSFET, and workable at 250V circuit.

FD2203S has built-in under-voltage (UVLO) protection to prevent the power tube at low voltage to work, and also for improving efficiency.

FD2203S has also built-in input signal filtering to prevent input noise. It can also prevent the short-circuit turning on of MOSFETs, and thus protect effectively the power devices

## Package



SOIC-8

## 250V Half-bridge Gate Driver

## Features

- Suspension absolute voltage :+250V
- Output current: +1.6A/-2.3A
- Input logic compatible: 3.3V/5V
- VCC/VBS Undervoltage protection (UVLO)
- High side output is in phase with the high side input
- Low side output is out of phase with the low side input
- Cross-conduction prevention
- Built-in 250ns dead time zone
- Channel matching for high and low side

## Application

Motor drive

DC-DC converter

## 1. Absolute maximum rating (Unless otherwise noted, all pins refer to COM as a reference point)

Parameter	Symbol	Range	Unit
High-side float absolute voltage	$V_B$	-0.3~275	V
High-side floating offset voltage	$V_S$	$V_B-25 \sim V_B+0.3$	V
High-side output voltage	$V_{HO}$	$V_S-0.3 \sim V_B+0.3$	V
Low-side supply voltage	$V_{CC}$	-0.3~25	V
Low side output voltage	$V_{LO}$	-0.3~ $V_{CC}+0.3$	V
Logic input voltage (HIN, LIN*)	$V_{IN}$	-0.3~ $V_{CC}+0.3$	V
Offset voltage slew rate range	$dV_S/dt$	$\leq 50$	V/ns
Power dissipation @ $T_A \leq 25^\circ\text{C}$	SOIC-8 $P_D$	$\leq 0.625$	W
Thermal resistance, junction to the ambient	SOIC-8 $R_{thJA}$	$\leq 200$	$^\circ\text{C/W}$
Junction temperature range	$T_j$	$\leq 150$	$^\circ\text{C}$
Storage temperature range	$T_{stg}$	-55~150	$^\circ\text{C}$

### Note:

- 1: Do not exceed  $P_D$  under any circumstances
- 2: Voltage exceeding absolute maximum ratings may damage the chip.

## 2. Recommended working conditions (All voltages are referenced to COM)

Parameter	Symbol	Min	Max	Unit
High-side float absolute voltage	$V_B$	$V_S+8$	$V_S+20$	V
High-side floating offset voltage	$V_S$	-2	250	V
High-side output voltage	$V_{HO}$	$V_S$	$V_B$	V
Low-side supply voltage	$V_{CC}$	8	20	V
Low side output voltage	$V_{LO}$	0	$V_{CC}$	V
Logic input voltage (HIN, LIN*)	$V_{IN}$	0	$V_{CC}$	V
Environment temperature	$T_A$	-40	125	$^\circ\text{C}$

### Note:

1. When  $V_S$  is (COM-2V) to 250V, HO works normally. When  $V_S$  is (COM-2V) to (COM- $V_{BS}$ ), the HO logic state is maintained.
2. When  $V_S$  is (COM-50V) and transient negative voltage is 50ns, HO can work as usual.
3. The reliability of the chip could be affected if it operates with long-term in the recommended working conditions.

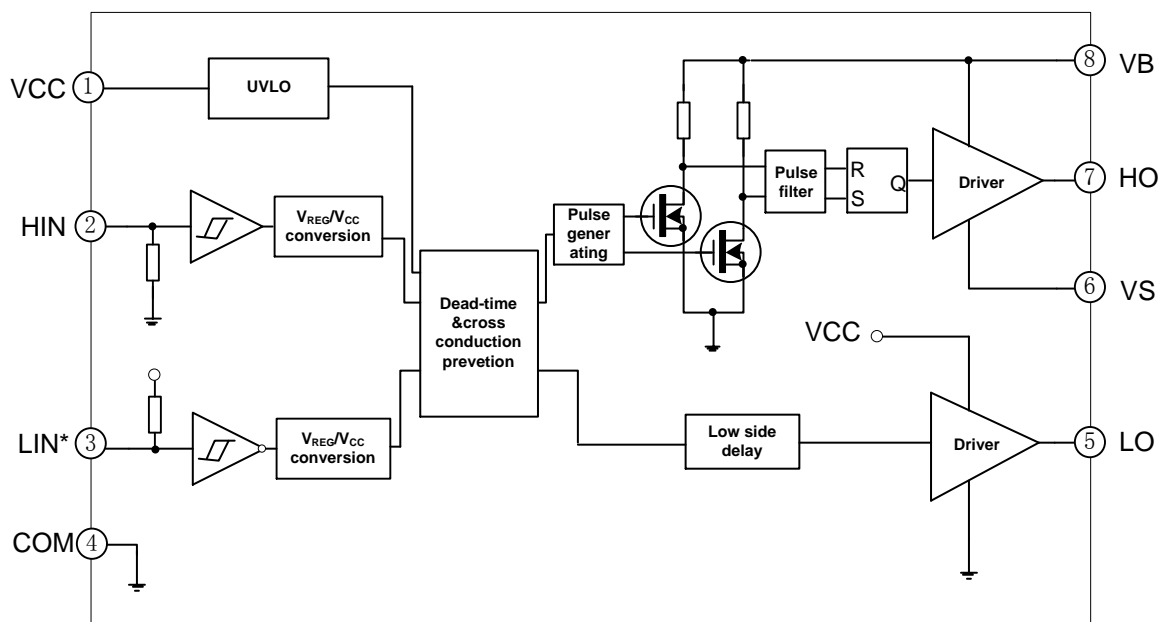
**3. Static electrical parameters** ( $T_A = 25^\circ\text{C}$  ,  $V_{CC}=V_{BS}=15\text{V}$  ,  $V_S=\text{COM}$ , Unless otherwise specified,)

Parameter	Symbol	Conditions	Min	Typical	Max	Unit
High level threshold input voltage	$V_{IH}$		2.4	--	--	V
Low level threshold input voltage	$V_{IL}$		--	--	0.8	V
$V_{CC}$ undervoltage protection trip voltage	$V_{CCUV+}$		6.3	6.9	7.5	V
$V_{CC}$ undervoltage protection reset voltage	$V_{CCUV-}$		5.9	6.5	7.1	V
$V_{CC}$ Undervoltage protection hysteresis voltage	$V_{CCUVH}$		0.2	0.4	--	V
$V_{BS}$ Undervoltage protection trip voltage	$V_{BSUV+}$		6.3	6.9	7.5	V
$V_{BS}$ Undervoltage protection reset voltage	$V_{BSUV-}$		5.9	6.5	7.1	V
$V_{BS}$ Undervoltage protection hysteresis voltage	$V_{BSUVH}$		0.2	0.4	--	V
Leakage current of suspended power supply	$I_{LK}$	$V_B=V_S=250\text{V}$	--	1.0	10.0	$\mu\text{A}$
$V_{BS}$ Static current	$I_{QBS}$	$V_{IN}=0\text{V}$ 或 $5\text{V}$	--	140	250	$\mu\text{A}$
$V_{BS}$ operate current	$I_{PBS}$	$f_{HIN}=20\text{kHz}$	--	140	250	$\mu\text{A}$
$V_{CC}$ Static current	$I_{QCC}$	$V_{IN}=0\text{V}$ 或 $5\text{V}$	--	460	700	$\mu\text{A}$
$V_{CC}$ operate current	$I_{PCC}$	$f_{IN}=20\text{kHz}$	--	460	700	$\mu\text{A}$
LIN* High-level input bias current	$I_{LIN+}$	$V_{LIN+}=0\text{V}$	--	20	40	$\mu\text{A}$
LIN* Low-level input bias current	$I_{LIN-}$	$V_{LIN+}=5\text{V}$	--	--	2	$\mu\text{A}$
HIN High-level input bias current	$I_{HIN+}$	$V_{HIN}=5\text{V}$	--	20	40	$\mu\text{A}$
HIN Low-level input bias current	$I_{HIN-}$	$V_{HIN}=0\text{V}$	--	--	2	$\mu\text{A}$
High-level output voltage	$V_{OH}$	$I_O=20\text{mA}$	--	0.09	0.16	V
Low-level output voltage	$V_{OL}$	$I_O=20\text{mA}$	--	0.03	0.06	V
High-level output short-circuit pulse current	$I_{OH}$	$V_O=0\text{V}$ , $\text{PWD}\leq 10\mu\text{s}$	1.1	1.6	--	A
Low-level output short-circuit pulse current	$I_{OL}$	$V_O=15\text{V}$ , $\text{PWD}\leq 10\mu\text{s}$	1.6	2.3	--	A
$V_S$ static negative voltage	$V_{SN}$		--	-6.0	--	V

**4. Transient electrical parameters** ( $T_A = 25^\circ\text{C}$ ,  $V_{CC} = V_{BS} = 15\text{V}$ ,  $C_L = 1000\text{pF}$ ,  $V_S = \text{COM}$ , unless otherwise specified)

Parameter	Symbol	Condition for texting	Min	Typical	Max	Unit
Output rising edge transmission time	$t_{on}$	$C_L = 1000\text{pF}$	--	350	520	ns
Output falling edge transmission time	$t_{off}$	$C_L = 1000\text{pF}$	--	100	150	ns
Output rising time	$t_r$	$C_L = 1000\text{pF}$	--	12	--	ns
Output falling time	$t_f$	$C_L = 1000\text{pF}$	--	8	--	ns
Dead-time	DT		--	250	370	ns
High-low side delay match	MT		--	--	50	ns

**5. Circuit diagram**



## 6. Chip pin configuration

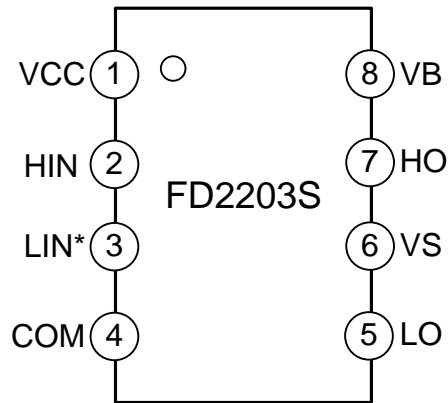
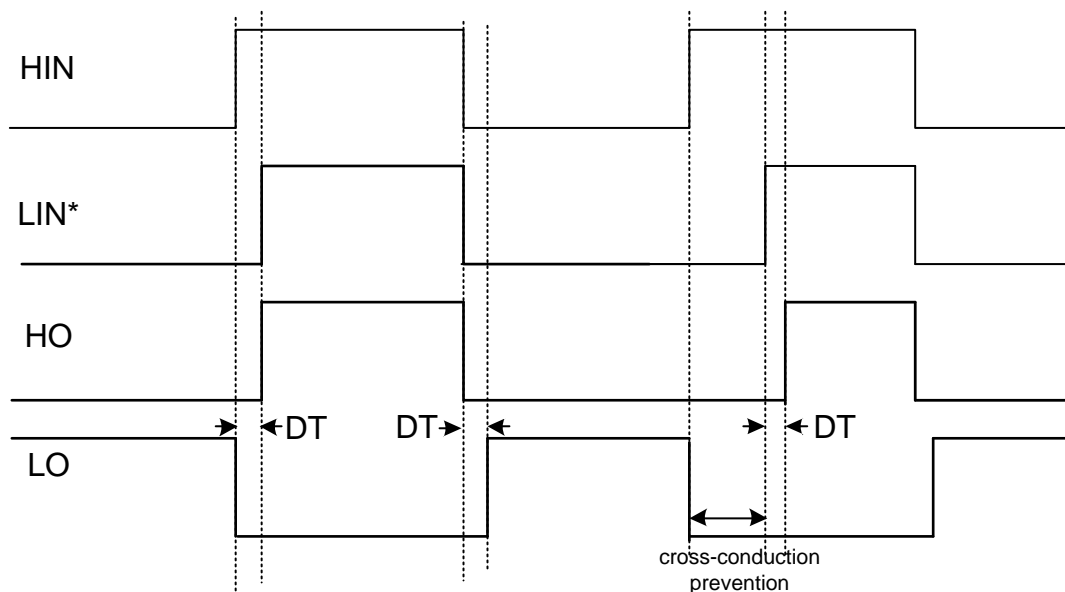


Figure 6-1 Package pin diagram

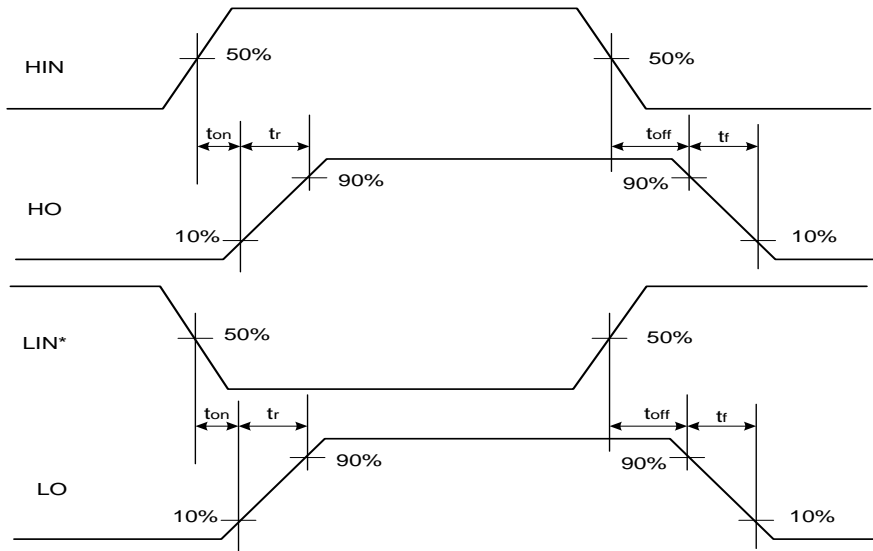
Table 6-1 Package pin

Pin no.	Pin name	Pin description
1	VCC	Low-side supply voltage
2	HIN	High-side input
3	LIN*	Low-side input
4	COM	Ground
5	LO	Low-side output
6	VS	High-side floating offset voltage
7	HO	High-side output
8	VB	High-side float absolute voltage

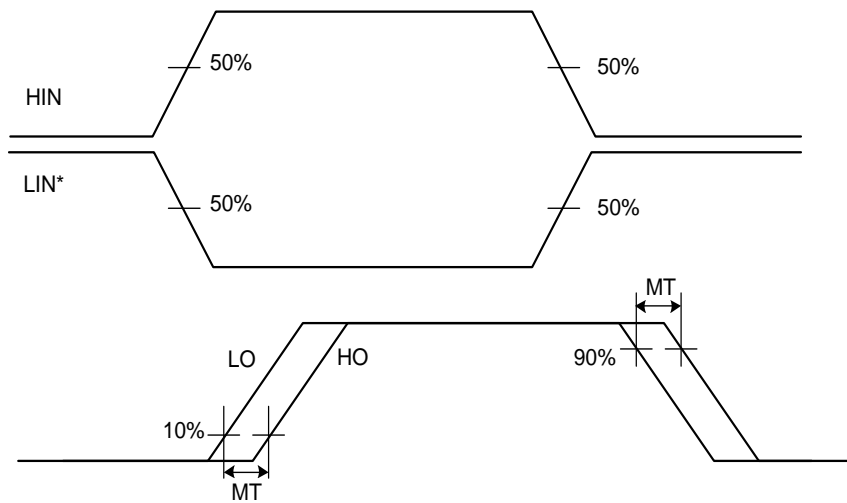
## 7. Logic timing diagram



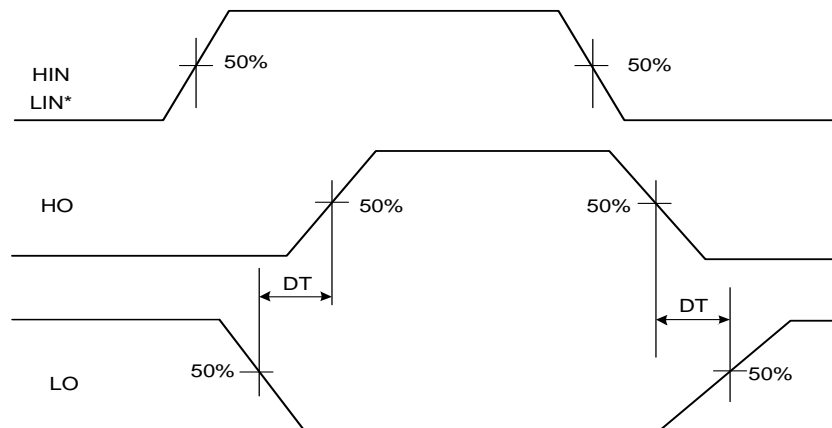
## 8. Switching time test standards



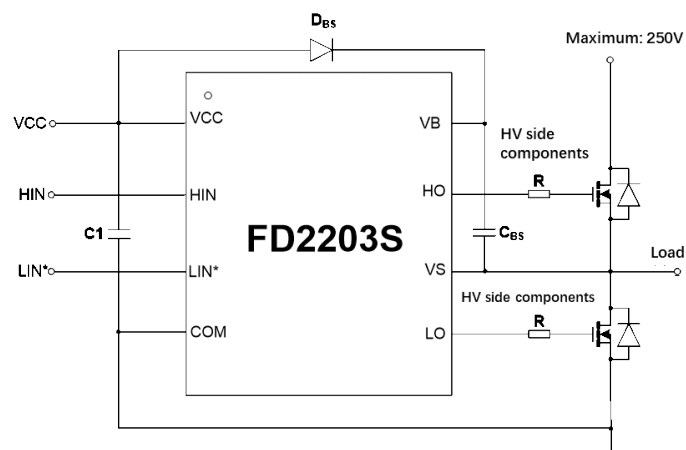
## 9. Transmission time matching test standards



## 10. Dead time test standards



## 11. Typical application circuit



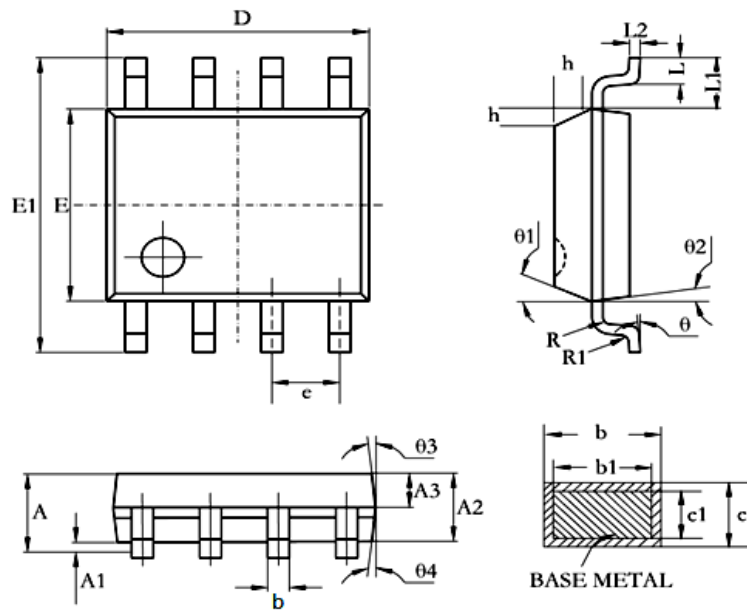
C1: Power filter capacitor, according to the circuit can choose  $1 \mu\text{F} \sim 100 \mu\text{F}$ , as close to the chip pin as possible.

R: Gate drive resistor, and the resistance depends on the device being driven.

D<sub>bs</sub>: Bootstrap diodes. It should be selected for high reverse breakdown voltage Schottky diodes.

C<sub>bs</sub>: Bootstrap capacitors. Ceramic capacitors or tantalum capacitors should be selected, according to the circuit can choose  $1 \mu\text{F} \sim 50 \mu\text{F}$ . The capacitor should be as close as possible to the chip pin.

**Note:** The above circuits and parameters are for reference only. The actual application circuit should be designed with the measured results in setting the parameters.

**12. Package size ( SOIC-8 )**


Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min	Nom	Max	Min	Nom	Max
A	1.36	1.55	1.75	0.053	0.061	0.069
A1	0.10	0.15	0.25	0.004	0.006	0.010
A2	1.25	1.40	1.65	0.049	0.055	0.065
A3	0.50	0.60	0.70	0.020	0.024	0.028
b	0.38	-	0.51	0.015	-	0.020
b1	0.37	0.42	0.47	0.015	0.017	0.019
c	0.17	-	0.25	0.007	-	0.010
c1	0.17	0.20	0.23	0.007	0.008	0.009
D	4.80	4.90	5.00	0.189	0.193	0.197
E1	5.80	6.00	6.20	0.228	0.236	0.244
E	3.80	3.90	4.00	0.150	0.154	0.157
e	1.27BSC					
L	0.45	0.60	0.80	0.018	0.024	0.031
L1	1.04REF					
L2	0.25BSC					
R	0.07	-	-	0.003	-	-
R1	0.07	-	-	0.003	-	-
h	0.30	0.40	0.50	0.012	0.016	0.020
θ	0°	-	8°	0°	-	8°
θ1	15°	17°	19°	15°	17°	19°
θ2	11°	13°	15°	11°	13°	15°
θ3	15°	17°	19°	15°	17°	19°
θ4	11°	13°	15°	11°	13°	15°

Product number	Package	Marking	Packing	Quantity
FD2203S	SOP8	FD2203S	Tape & Reel	3000



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