FPGA Implementation of Quasi-BLDC Drive

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***Abstract*—For the reduction of acoustic noise and vibration generated in self-sensing brushless dc motor operation, a self-sensing quasi brushless DC drive (QBLDC) mode is presented. The structure of the drive and the related algorithms are introduced in detail in the paper. The drive can be implemented on field programmable gate arrays (FPGA). The performance of the drive presented has been confirmed by the testing results of the spindle motor used in hard disk drive.**

***Index Terms*—Self-sensing, BLDC, Spindle Motor, Acoustics and FPGA.**

I. Introduction

The introduction of high energy permanent magnet materials coupled with the increasing concerns for power efficiency has opened the gateway for Permanent Magnet Synchronous Motor (PMSM). The benefits of using PMSM include power density and high efficiency and low acoustics noise. As such, it has become an attractive option for industrial applications, such as Hard Disk Drives (HDD). The motor deployed HDD are a sub category belonging to PMSM, commonly known as Brushless DC Motor (BLDCM). Compared to PMSMs, this kind of BLDCM has several unique features. The rotor of BLDCMs has got surface-mounted permanent magnet constructing a smooth-air-gap machine. As such, reluctance torque contributed by inductance variations can be neglected. In addition, the rotor utilizes fractional-slots which in turn make the cogging torque negligible. These, together with other features, such as sinusoidal/ trapezoidal back-emfs and a well symmetrized three-phase structure, create an unique PMSM or a BLDCM. [1]

In PMSM drives, the motor usually has a rotor position sensor, such as encoder or resolver. In BLDCM drive, usually three hall effect sensors are used as rotor position sensors. However, these sensors are undesirable as they incur additional cost and space. As such, self-sensing, or sensorless control, is often being deployed for the BLDCM drives. There are many categories of self-sensing solutions [1]-[3], such as the back-EMF voltage sensing, back-EMF integration, flux estimation and detection of freewheeling diodes conduction. In HDD, the self-sensing operation is accomplished by the utilizing the back-EMF zero crossing points (ZCPs) as rotor position information. In a BLDC drive, each gate turns on for 120° and for each phase, there will be two silent periods, each of 60°, where the terminals are floating. It is during the silent phase that the ZCPs will occur and to detect these ZCPs, a common method is to create a virtual neutral point and compare it to the voltage terminal. And the resulting signal will have ZCPs equivalent to the back-emf ZCPs. However, due to gate commutation, spikes occur and these will result in false ZCPs.

Back-emf based methods, however, fail during starting where the back-emf are zero or small. As such, during starting, the motor is driven open loop with six-stepping on a skewed frequency to a speed, ω_{co}. At ω_{co}, the back-emf is sufficiently large to be detected and all voltage terminals are floated for back-emf detection. However, due to the removal of gating signals, the motor will be decelerating and this will result in declining back-emfs. Thus, in the determination of ω_{co}, it is tuned higher to take into account of this decline. Beyond ω_{co}, the system advances to the self-sensing BLDC drive.

In BLDC drive, during the 120° conduction segment, the goal is to inject rectangular stator phasor currents during that period. However, the motor being inductive, voltage spikes will occur during commutation. These spikes are undesirable as they are a source of both electrical and mechanical noise, and vibration.

In recent years, owing to the progress of VLSI technology, the field programmable gate array (FPGA) has gained world wide acceptance. It has traditionally been perceived as a essential platform for Application Specific Integrated Circuit (ASIC) prototyping. However, in recent years, it has gained significant market share in end-product solutions as fundamentally, FPGA offers fast time to market, low design/manufacturing cost and risk, extremely high processing performance, and programmability.

The research goal of this paper is to design a Self-Sensing Quasi-BLDC (QBLDC) Drive on FPGA. The FPGA design comprises of

(1) an innovative back-emf based method for rotor position detection with zero delay;
(2) a six step δ° masked open loop starting for bumpless crossover to BDLC/QBLDC drive, and
(3) a QBLDC drive for reduction of acoustics and vibration generated in the motor operation.

In (1), the proposed method takes an integrative approach in back-emf zero-crossing-points (ZCP) detection and BLDC/QBLDC drive implementation. Heuristic logic is adopted in the implementation and accurate BDLC/QBLDC drive with zero delay ZCP detection for wide speed range is achieved. In (2), the proposed methodology proposes a novel gate signal masking on a six step open loop self starting enabling

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back-emf detection possible without a complete removal of gating signals. The strategy offers the advantages of i. an earliest possible crossover while making no assumption on the crossover frequency, ii. smooth crossover as the motor rotation is continued iii. continuance of frequency skewing during detection. In (3), the proposed drive aims to reduce the drive acoustics and runout by the reduction of the drive current spikes. It uses a trapezoidal drive instead of rectangular drive for gating. By utilizing such an approach, the current spikes are reduced and its effect on acoustics and vibration are reduced.

II. Brushless DC (BLDC) Operation

In a BLDC drive, the motor is typically driven by a three-phase inverter circuit as shown in Fig. 1. It consists of six power semiconductor transistors with a protection diode connected in parallel to each of these transistors.

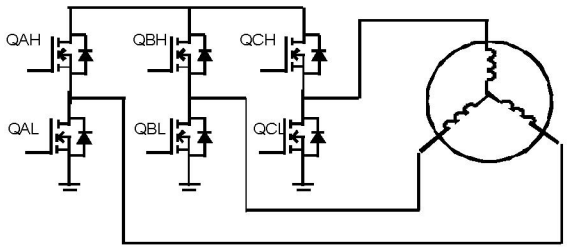

Fig. 1. Bridge Circuit for BLDC Drive

Each transistor is gated by a 120°-conduction drive, in which each gate turns on for 120 electrical degrees in each cycle. Commutation occurs at every 60 electrical degrees of rotation in the sequence QAH, QCL, QBH, QAL, QCH and QBL. For maximum torque production, the gating with respect to the back-emf is given in Fig. 2. For each phase, there will be two unexcited 60° periods, where the voltage terminals are floating or unexcited. During this unexcited phase, the phase voltage gives the phase back-emf. Optimally, the zero crossing points (ZCPs) of the phase back-emfs should occur mid-way in the silent period. These ZCPs represent position information and it's based on this that self-sensing operation using back-emf ZCP detection is established.

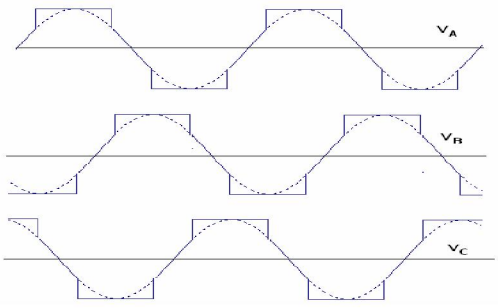

Fig. 2. Terminal Voltage waveforms

III. Self-Sensing Operation Using Back-EMF ZCP Detection

As highlighted, during the unexcited phase, the phase voltage gives the phase back-emf which would encompass the ZCP. In the detection of ZCP, however, the entire phase voltage is not required as at the instants of ZCPs, the terminal voltages would be equal to the neutral voltage. Consequently, the detection of ZCPs is equivalent to the detection of the instants whereby VAN or VBN or VCN equals to zero. Whilst the terminal voltages are available, the neutral voltage might not be available. A common method is to reconstruct a "virtual" neutral which provides a equivalence to the actual neutral. To derive the ZCP signals, the terminal voltage is thus compared to the virtual neutral voltage and the comparison will provide signals with ZCPs corresponding to the back-emf ZCPs. Fig. 3 illustrates the notion pictorially depicting the terminal voltages comparison with the virtual neutral constructed.

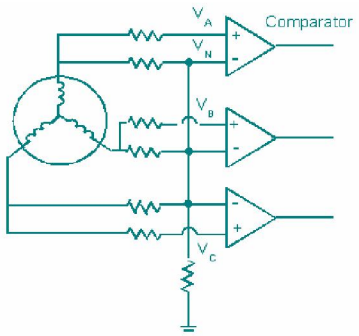

Fig. 3. ZCP Detection Circuit

Practically, however, the simplistic topology fail as voltage spikes will occur for every commutation. As a result, false ZCPs are immersed amongst true ZCPs. This problem has been well documented and researched, among which many methods center on the usage of filters which inevitably result in phase delays.

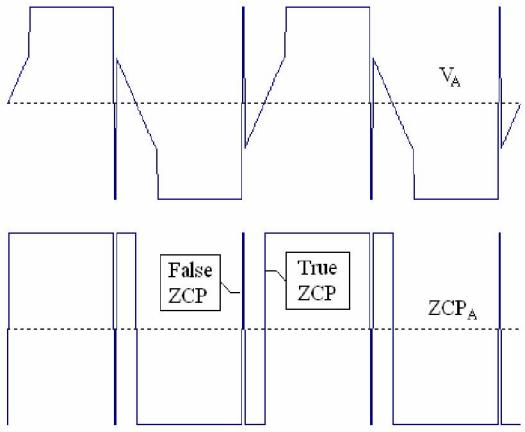

Fig. 4. Comparator Waveforms

Most of the methods focus on the removal or exclusion of these false ZCPs when they occur. In this proposed method, an adoption of an integrative Zero Delay ZCP Detection - BLDC drive is utilized.

In a BLDC drive, a commutation occurs 30 electrical degrees (30°) after every true ZCP is detected. To estimate this 30°, the following algorithm is proposed.

a. A global free running counter is implemented in the design and latches are used to store the counter counts for all the ZCPs.
b. Positive edge transitions will be used to latch the 0°, 120° and 240° ZCPs counter counts whereas negative edge transitions will be used to latch the 60°, 180° and 300° ZCPs counter counts.
c. 30° time lag is to be estimated using the 60° time lapse from the last ZCP to latest ZCP detected. For example, to estimate the 30° time lag after the occurrence of 0° ZCP, the 30° time lag would be equivalent to the point whereby the counter has further increased by ½ × (Latch0° - Latch300°) since the 0° ZCP. The factor of ½ is easily accomplished by a single bit right shift of (Latch0° - Latch300°).

At this juncture, the algorithm, however, too suffers from the presence of false ZCPs, resulting in incorrect counter counts being latched. However, achieving zero delay ZCP detection is only possible if all ZCPs are taken as true as when it occurs. This constraint implies that the latching must be done for all ZCPs, true or false.

This constraint can be elegantly respected by the inclusion of false ZCP avoidance within the BLDC drive algorithm. An unique property derived from the signals is during the 30° time lag for commutation, after an active ZCP detection, inactive ZCPs should never occur during the 30° time lag. For example, 0° ZCP counter count will be latched by positive or rising edge ZCP transitions. However, in the 30° time lag, inactive negative or falling edge ZCP will not occur if the preceding active ZCP is true. Hence, in the presence of an inactive ZCP during the 30° time lag interval, the interval will be made inactive, latch will be restored to its previous count and active edge ZCP transition is awaited. As an additional level of heuristic control, it can be observed that apart from satisfying the 30° time lag, commutation should occur only at the active level. Thus, the integrated algorithm becomes

a. A global free running counter is implemented in the design and latches are used to store the counter counts for all the ZCPs.
b. Positive edge transitions will be used to latch the 0°, 120° and 240° ZCPs counter counts whereas negative edge transitions will be used to latch the 60°, 180° and 300° ZCPs counter counts. 30° time lag is to be estimated using the 60° time lapse from the last ZCP to latest ZCP detected.
c. Occurrence of inactive edge transitions will be reset ZCP counter counts to its previous counter values. Negative edge transitions will trigger a reset of the 0°, 120° and 240° ZCPs counter counts whereas positive edge transitions will trigger a reset of the 60°, 180° and 300° ZCPs counter counts.
d. If the current count minus the ZCP latched count equals to the estimated 30° time lag and current ZCP signal level remains active, commutation occurs. Waiting for 60° ZCP counter counts commences.
e. Pictorially, the algorithm is provided in Fig. 5 and its schematic provided in Fig. 6.

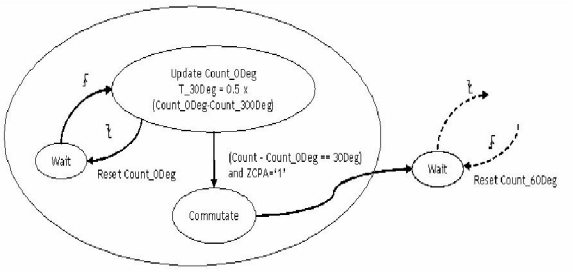

Fig. 5. Flowchart of proposed algorithm

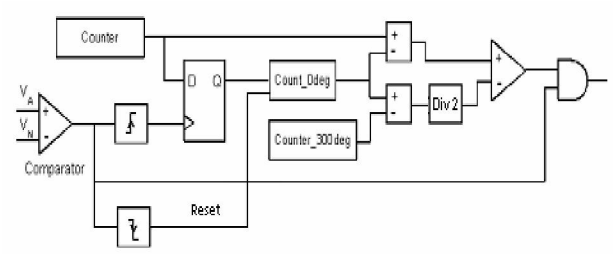

Fig. 6. Schematic of integrated Zero Delay ZCP Detection

IV. Crossover From Six Stepping to Self-Sensing BLDC Operation

In self-sensing bldc operation, position feedback from back-emf ZCPs is not available at starting or low speeds. The motor is typically open loop started from standstill in a six stepping mode with a skewed frequency to ω_{co} speed. At ω_{co}, two conditions must be met; (i) back-emf is sufficiently large to be detected (ii) ZCPs occur during the unexcited phase of gating. Fig. 7 gives the gating signals with respect to the ZCP signals in an ideal crossover.

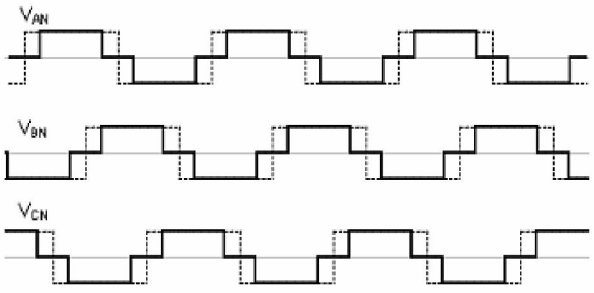

Fig. 7. Gating & Back-Emf Waveforms

However, practically, it is tuned to achieve the gating and ZCP phasor relationship as in Fig. 7. Such an approach, apart from requiring time and effort, is system dependent. Another approach is to switch off all the gates and detect the ZCPs as soon as the phase currents decrease to zero. This method, though simplistic, causes the motor to decelerate and its corresponding back-emf to diminish which inevitably requires a higher ω_{co}. Furthermore, the deceleration of the motor will cause a "bump" in the crossover. In addition, in the event of a failure, restarting is difficult as it is to be restarted on a decelerating motor.

In this proposed methodology, a novel gate signal masking technique is utilized, making back-emf detection possible without a complete removal of gating signals. To provide insights into this, it would be beneficial if the phenomenon at six stepping is better understood. During open loop six stepping, generally, the wave will not be that as intended. Typically, the drive is over driven to provide a higher starting torque for acceleration as well as overcoming frictional, viscous torque. The phasor relationship between the gating and backemf will differ by a larger angle than that seen in Fig. 7. Generally, in an extreme case, the phasor relation is similar to that illustrated in Fig. 8.

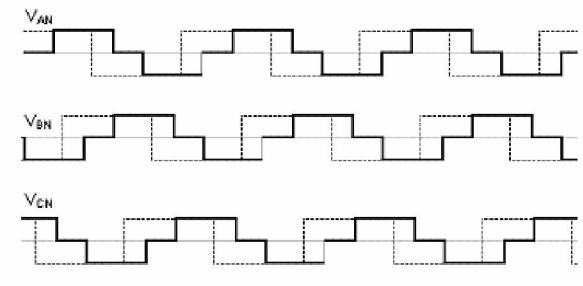

Fig. 8. Gating & Back-Emf Waveforms

As mentioned, to extract the ZCPs, the system can be tuned or all the gates turned off. In this method, this matter can be elegantly rectified by performing gate masking.

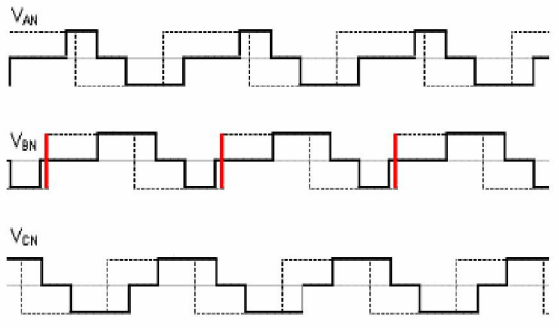

Fig. 9. Gating & Back-Emf Waveforms with δ masking, δ = 60°

The motor is similarly started on a six-stepping mode. However, the gating signals are masked out an arbitrary angle, δ, as soon as the motor rotates. This will increase the silent phase window and for any $\delta \geq 60°$ this will guarantee at least one ZCP detection. Fig. 9 illustrates the possible detection of a ZCP with gate signals masking.

In doing so, since only 60° of the gating signals are masked out, the inertia of the motor will keep rotation going in contrast with the complete removal of gating signals. This means even if the window/back-emf is missed, the same back-emf amplitude is available for detection after a 300° angle rotation. Thus, since the motor is not made to decelerate, a smooth and more robust transfer is possible. In addition, the assumption that the back-emf is large enough for detection is no longer necessary as such strategy allows the skewing of frequency to be continued till back-emf is large enough for ZCP to be detected.

An extension of the method is to mask the gating signals by δ=120°. In doing so, an additional 60° window will make two ZCPs available for detection. This will greatly reduce the possibility of erroneous detection since dual detection is provided. However, it must be noted that, by setting up gate masking, the starting torque will be reduced. Nevertheless, it should not be a concern as the motor is commonly overdriven at starting.

V. Self-Sensing Quasi-BLDC (QBLDC) Operation

In BLDC operation, for torque production, the transistors are commutationally switched as shown in Fig. 10 to provide rectangular stator currents. While the objective is to inject phasor rectangular currents, in reality, current waveforms as shown in Fig. 11 are injected. The reason being, the motor is inductive in nature will accumulate energy when driven. During commutation, the interruption of inductive currents will result in current spikes. There are two types of spikes belonging to two different sources. For those spikes at the side (in-phase spikes), they are to the turning on and off of its corresponding gates, whereas for the spikes at the middle of the rectangular currents (adjacent-phase spikes), they are due to the turning on and off of its adjacent gates. Nevertheless, both of these spikes are undesirable as they are a source of noise and vibration.

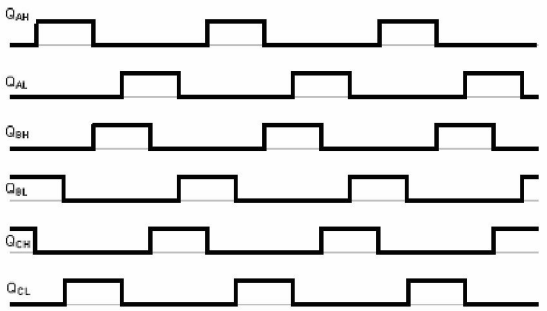

Fig. 10. BLDC Gating Signals

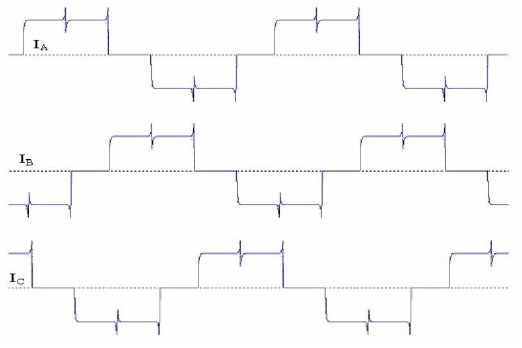

Fig. 11. BLDC Phase Currents

To reduce these spikes a quasi-BLDC drive is proposed. In this drive, trapezoidal phase voltages as shown in Fig. 12 are to be achieved instead of rectangular phase voltages. Execution wise, it means to compare a trapezoidal reference to a triangular signal.

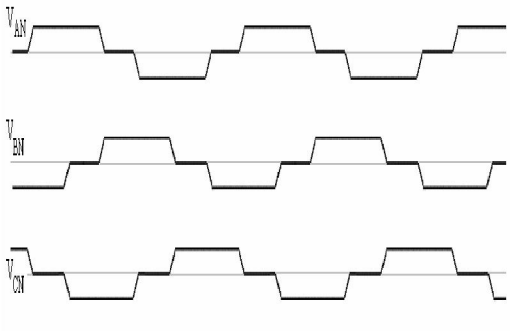

Fig. 12. QBLDC Phase Voltages

The purpose of such a drive is to control the injection and withdrawal of phase currents to reduce the in-phase spikes. On a single phasor topology, it works fine and these spikes can be significantly reduced. However, in a three phase topology, such a method gives rise to a peculiar development. The in-phase spikes will reduce but adjacent-phase spikes will increase. In-phase spikes can be reduced as voltages are slowly injected. However, due to a three phase topology, the overlap in gating between the commutating phases will result in an increased current in the non-commutating phase. This non-commutating phase, then, suffers from adjacent-phase spikes. This is illustrated in

Fig. 13 under (I). In the turning off of phase A and turning on of phase B, there will be instants where both QAH and QBH are turned on. This implies a spike in current in phase C.

To deal with this problem, the PWM trapezoidal switching in (II) is proposed. In this proposed switching, to turn on a gate, the trapezoidal reference and the normal PWM is used. However, to turn it off, the logic inverse of the adjacent sequential gating signal is used. For example, QBH is turned on following QAH is turned off. Therefore, to turn off QAH, the NOT of QBH is applied. In doing so, at any one time, only one gate from the upper leg is turned on. This will ensure that the current following through QCL remains relatively constant and also the currents through QAH and QBH are respectively decreasing and increasing slowly.In self-sensing bldc operation, position feedback from back-emf ZCPs is not available at starting or low speeds. The motor is typically open loop started.

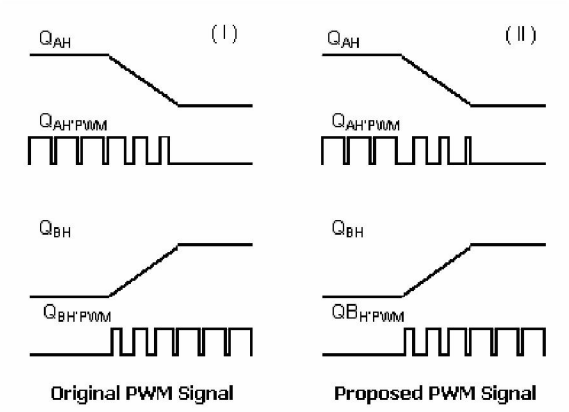

Fig. 13. PWM Signals for QBLDC Drive

VI. FPGA Implementation and Experimental Results

The overview of the FPGA implementation is provided in Fig. 14. Each of the modules have been coded with VHDL and is implemented on a XC4VFX12, a Xilinx Virtex-4 FX FPGA Device. The design is synthesized, implemented and simulated entirely on Xilinx ISE 8.1. The design was then used to drive a Hard Disk Spindle.

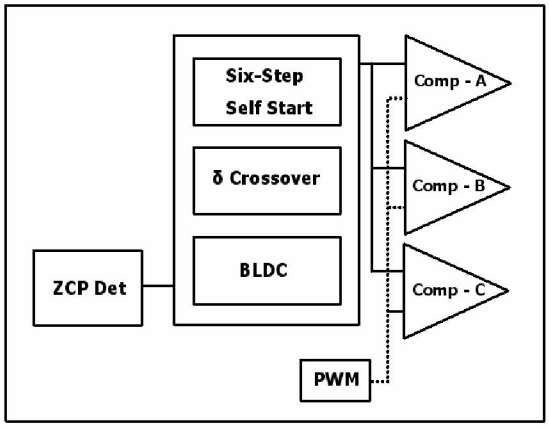

Fig. 14. Block Diagram of FPGA Design

Fig. 15 gives the terminal voltage waveform VA, the virtual neutral VN, the ZCP waveform from a comparator and IA, the phase current. It can be observed that false ZCP are not treated as true and the true ZCP are in fact used for commutation.

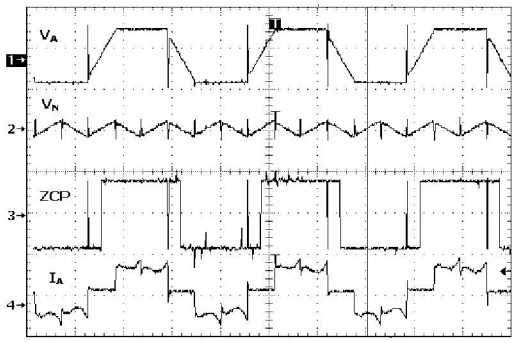

Fig. 15. Waveforms for BLDC Drive

In the implementation of QBLDC, the BLDC entity is swapped with QBLDC. The current waveform comparison between the two drives are given in Fig. 16.

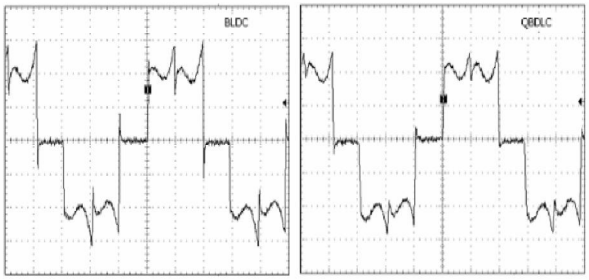

Fig. 16. Current Waveforms for BLDC & QBLDC Drive

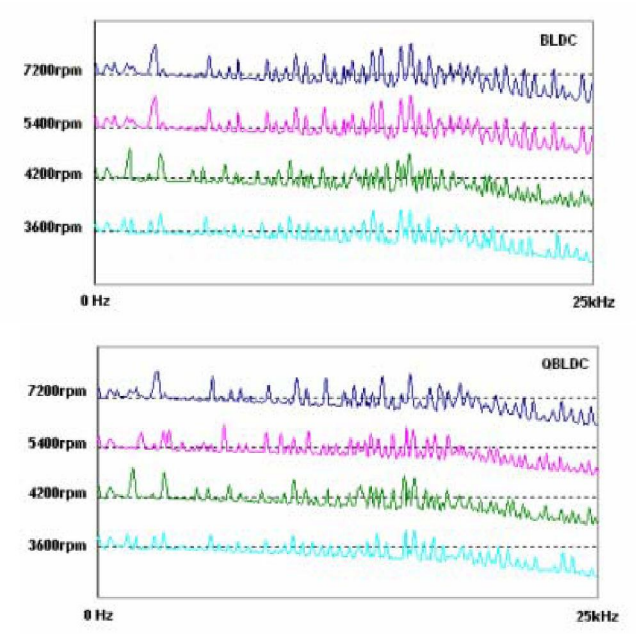

Fig. 17. Noise Waveforms for BLDC & QBDLC Drive

As mentioned, BLDC drive given gives as spiky current and QBDLC drive has reduced the spikes by 40%. Fig. 17 shows the acoustics noise captured for four different operating speeds with Acoustics Chamber. It can be seen that QBLDC gives a lower noise floor compared to BLDC. This is intuitive as a spike is considered to be rich in frequencies and a reduction will result in a reduction of noise frequency across a wide range.

VII. Conclusions

In this paper, a self-sensing quasi brushless DC drive mode for brushless dc motors is presented. This drive comprises of

(1) an innovative zero delay back-emf based method for rotor position detection;
(2) a six step δ° masked open loop starting for bumpless crossover to BDLC/QBLDC drive;
(3) a QBLDC drive for reduction of acoustics and vibration.

By integrating all the schemes put forward, the drive is implemented on field programmable gate arrays. Tests results showed that, when the presented self-sensing drive is used, the voltage spikes induced by the commutation can be reduced significantly, and the acoustic noise and vibration of the BLDCM can thus be observably reduced. These testing results prove the effectiveness of the proposed drive.

Acknowledgement

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