Design of A/D Converters with Hierarchic Networks

Teck Seng Low, *Senior Member, IEEE,* and Chao Bi

***Abstract*— A methodology for designing Analog to Digital (A/D) converters based on a hierarchic network is explored. The principle of this methodology and design procedure are presented. The characteristics and performances of the converter are compared with the converter based on the Hopfield network. Two circuit models for the A/D converters are described in this paper. As a hierarchic network is used, the A/D converters designed have no local minima in their operation. With the method proposed in the paper, high bit number A/D converters can be easily designed, and the converters designed are fast in signal conversion and stable in operation.**

NOMENCLATURE

- V_c The comparator output voltage when its inverting input voltage is higher than 0 (here, V_c is a negative value).
- V_{inet} The net voltage of the ith comparator inverting input node.
- V_m The maximum voltage which the converter can convert.
- V_m^* The normalized V_m (for a 4-bit A/D converter, $V_m^* = 15$).
- V_{o_i} The jth bit output voltage of the converter (it is a negative value)
- V_r The reference voltage (it is a negative value).
- V_x The input signal voltage (it is a positive value).
- V_x^* The normalized V_x (for a 4-bit A/D converter, $V_x^* = (15/V_m) \cdot V_x$).
- Y_{ij} The conductance connecting the inverting input of the ith comparator to the output of the jth comparator.
- Y_{ij}^* The normalized conductance of Y_{ij} (for a 4-b A/D converter, $Y_{ij}^* = (15/V_m) \cdot Y_{ij}$).
- Y_{ir} The conductance connecting the inverting input of the ith comparator to the reference voltage V_r.
- Y_{ix} The conductance connecting the input of the ith comparator to the input signal V_x.

I. INTRODUCTION

PRESENTLY, there are four types of A/D converters available commercially. They are

1) counting type A/D converters;
2) successive approximation type A/D converters;
3) parallel comparator type A/D converters;
4) ratiometric type A/D converters.

Manuscript received January 6, 1995; revised June 18, 1995.

T. S. Low is with the Magnetics Technology Center, National University of Singapore, 0511, Singapore

C. Bi is with the R&D Centre, Western Digital (S) Pte Ltd., Singapore, 1646.

Publisher Item Identifier S 0278-0046(96)01273-7.

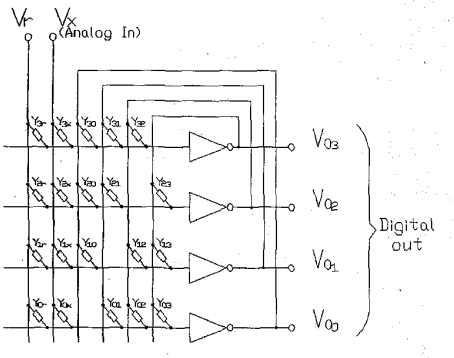

Fig. 1. The A/D converter based on the Hopfield network.

Counting A/D converters is lowest in conversion speed as it takes 2^N clock cycles for an N-bit conversion. The conversion speed is fastest in parallel comparator A/D converters but their circuits are complicated if the number of bits are high. Recently, some new innovative designs have been published. They include the application of neural networks to A/D converter designs. Designs based on the Hopfield network is one of them [1]. In this paper, we propose the use of a hierarchic network to design A/D converters. The converters based on this network have desirable and unique properties which may be useful in many applications. Their advantages include 1) speed, 2) simplicity, 3) not needing clock signals, and 4) having no local minima. In describing the designs of the A/D converter using hierarchic networks, the designs based on the Hopfield network is first discussed. Using this as the base for comparison, the designs of A/D converters with hierarchic networks by bit extension is described. The full hardware implementation of a 10-bit A/D converter is shown and its performance is presented.

II. THE A/D CONVERTER BASED ON A HOPFIELD NETWORK

The Hopfield network is a recurrent symmetric neural network which can be used to design A/D converters [1], [2], [5]. The circuit of a 4-bit converter based on the Hopfield network is shown in Fig. 1, where Y_{ij} is the conductance connecting the inverting input of the ith comparator to the output of the jth comparator and $Y_{ij} = Y_{ji}$. Its simple design makes the converter inexpensive and easy to be built.

The Hopfield network has feedback paths from their outputs back to their inputs and it has been proven that this recurrent symmetric network is stable [2]. Its response is dynamic, that is, after applying a new input, the output is modified and fed back to the input terminals. The output is then

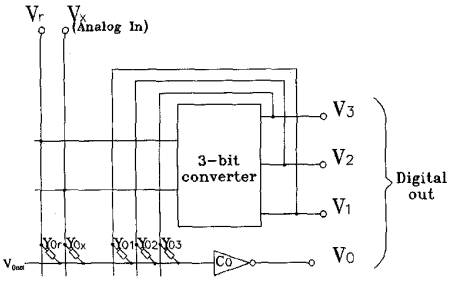

Fig. 2. Extending the bit number of an A/D converter.

modified, and the process is repeated. The iterations produce smaller and smaller output changes until eventually the outputs become constant. The Hopfield network has local minima. These minima require the converters to be reset before every conversion, or else the conversion error could be very large [2], [7]. This disadvantage limits the use of the converter in many high-speed applications.

In [4], it is noted that the symmetry bounded to the recurrent network is sufficient but not necessary for stability of the network. This indicates that A/D converters could be designed by using asymmetric networks, and the analysis in the following sections will also prove that this design is practical.

III. Extending the Bit Number of an A/D Converter

For convenience in analysis, we examine the possibility of extending a 3-bit A/D converter to a 4-bit one. An arbitrary 3-bit converter is chosen. The circuit of the extended bit is shown in Fig. 2. This circuit is formed by a comparator and a series of resistors and the circuit forms the lowest bit of the converter. The reference voltage, input voltage and all higher bit outputs are connected to the inverting input of the extended circuit, respectively, but the output of the extended bit circuit is not fed back to the input of the converter. Fig. 2 shows only the extended circuit which forms the lowest bit of the converter, so only Y_{0r}, Y_{0x}, Y_{01}, Y_{02}, and Y_{03} are shown in Fig. 3. The relation between output and input of the ith comparator is described by (1).

$$V_{o_0} = \begin{cases} 0, & V_{0\text{net}} < 0 \\ V_c, & V_{0\text{net}} \geq 0 \end{cases} \tag{1}$$

where V_{o_0} is the output voltage of the comparator C_o, $V_{0\text{net}}$ is the net voltage on the input terminal of C_o The curve of $V_{o_0}(V_x)$ is shown in Fig. 4.

In latter analysis we will assume that V_m, V_x and Y_{ij} have been normalized, that is, $V_m = V_m^*$, $V_x = V_x^*$ and $Y_{ij} = Y_{ij}^*$, unless otherwise stated, where V_m and V_x are the maximum voltage which the converter can convert and the input signal voltage, respectively.

In order to form the 0th bit of the A/D converter, $V_{o_0}(V_x)$ of the 0th comparator must satisfy the function shown in Fig. 3. Equation (2) can describe this condition.

$$V_{o_0} = \begin{cases} 0, & 2k \leq V_x < 2k+1 \\ V_c, & 2k+1 \leq V_x < 2k+2 \end{cases} \quad (k = 1, 2, \cdots, 7). \tag{2}$$

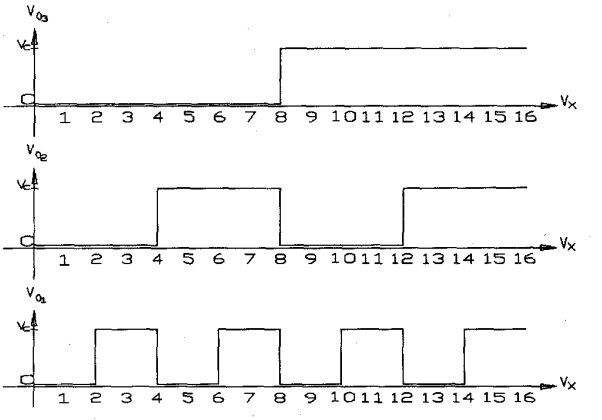

Fig. 3. Function of $V_{o_0}(V_x)$.

The 0th bit circuit has 5 unknown parameters: Y_{0x}, Y_{0r}, Y_{01}, Y_{02}, Y_{03}. When k in (2) changes from 0 to 7, 16 equations are yielded. It is clear that finding 5 parameters which can satisfy all these equations is difficult. To get the solution, an effective calculation method has to be found to performed the bit extension.

To obtain a practical solution for the bit extension, the properties of the curve $V_{o_0}(V_x)$ should be analyzed carefully before calculating for these parameters. With the comparator property shown in (1), the requirements described in (2) can be changed to the one described by (3).

$$V_{0\text{net}} \begin{cases} < 0, & 2k \leq V_x < 2K+1 \\ \geq 0, & 2k+1 \leq V_x < 2k+2. \end{cases} \tag{3}$$

Equation (3) is formed by a group of inequalities. To solve this equation, it is necessary to analyze $V_{0\text{net}}(V_x)$, shown in Fig. 2.

The curve $V_{0\text{net}}$ can be described by

$$V_{0\text{net}} = \frac{V_x \cdot Y_{0x} + V_r \cdot Y_{0r} + V_{o_1} \cdot Y_{01} + V_{o_2} \cdot Y_{02} + V_{o_3} \cdot Y_{03}}{Y_{0x} + Y_{0r} + Y_{01} + Y_{02} + Y_{03}}. \tag{4}$$

In (4), only V_x, V_{o_1}, V_{o_2}, and V_{o_3} are variables, but the latter three variables are also functions of V_x. The functions $V_{o_1}(V_x)$, $V_{o_2}(V_x)$ and $V_{o_3}(V_x)$ are shown in Fig. 4. Therefore,

$$V_{0\text{net}} = V_{0\text{net}}(V_x). \tag{5}$$

When V_x changes, in the region $V_x \neq k$ $(k = 0, 1, 2, \cdots, 15)$, all outputs bits of the converter remain constant. This case is deduced by differentiating (4) with respect to V_x.

$$V'_{0\text{net}}(V_x) = \frac{Y_{0x}}{Y_{0x} + Y_{0r} + Y_{01} + Y_{02} + Y_{03}}. \tag{6}$$

TABLE I
THE VALUES OF $D(k)$

k	2	4	6	8	10	12	14
D(k)/V_c	Y_1/Y_S	$(Y_2-Y_1)/Y_S$	Y_1/Y_S	$(Y_3-Y_2-Y_1)/Y_S$	Y_1/Y_S	$(Y_2-Y_1)/Y_S$	Y_1/Y_S

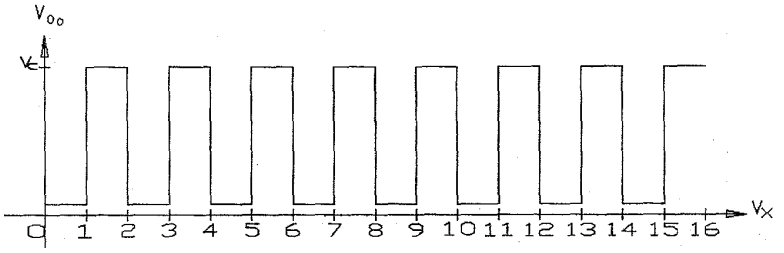

Fig. 4. Transfer function of the 3-bit A/D converter.

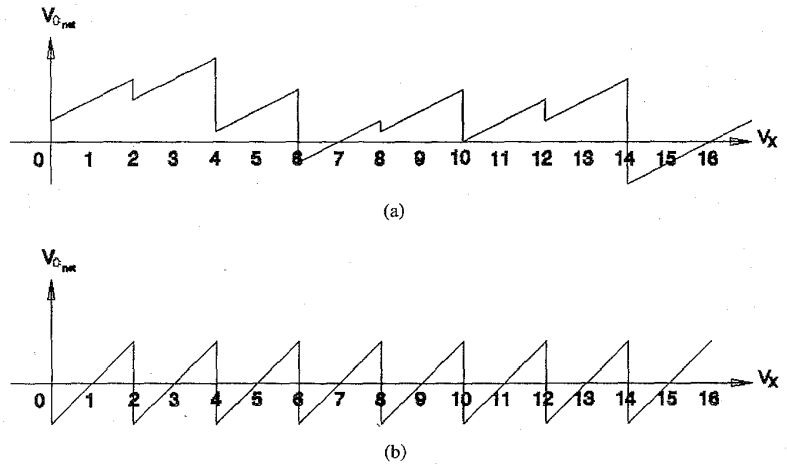

Fig. 5. The performance of $V_{0\text{net}}(V_x)$. (a) Equation (9) cannot be satisfied. (b) Equation (9) can be satisfied.

Equation (6) shows an important property of $V_{0\text{net}}(V_x)$:

The derivative of $V_{0\text{net}}(V_x)$ *in* (4) *is a constant,* Y_{0x} *if* $V_x \neq k$.

Another property of $V_{0\text{net}}(V_x)$ can be described by (7)

$$D(k) = \lim_{\varepsilon \to 0} \{V_{0\text{net}}(k+\varepsilon) - V_{0\text{net}}(k-\varepsilon)\}. \tag{7}$$

The results for different values of $V_x = k$ are shown in Table I.

Table I shows that if the condition described by (8) is satisfied and V_c is negative, $D(k)$ must be negative.

$$Y_i > \sum_{j=0}^{i-1} Y_j \tag{8}$$

The performance of $D(k)$ shows that

When V_x *increases continuously,* $V_{0\text{net}}$ *falls abruptly at points where* $V_x = 2k$.

These two properties of the function $V_{0\text{net}}(V_x)$ are shown in Fig. 5. The points on the curve at $V_x = (2k-1)$ $(k = 1, 2, \cdots, 8)$ can be adjusted by choosing different values for conductances Y_r and Y_{0i} $(i = 1, 2, 3)$. These conductances can be made to satisfy Eq. (9) to obtain the curve b shown in Fig. 5. In this way, the bit number extension will be can be made if the conductances Y_r and Y_{01} are known.

$$V_{0\text{net}}\big|_{V_x = 2K-1} = 0 \quad (k = 1, 2, \cdots, 8). \tag{9}$$

To calculate for the values of the conductances required, a matrix equation is set up with (4) and (9) for k varying from 1 to 8, as there are eight transitions for the lowest bit in a 4-bit A/D converter.

$$\mathbf{Y} \cdot \mathbf{V} = \mathbf{0} \tag{10}$$

where

$$\mathbf{Y} = \begin{bmatrix} 0 & 0 & 0 & Y_{0x} & Y_{0r} \\ Y_{01} & 0 & 0 & 3Y_{0x} & Y_{0r} \\ 0 & Y_{02} & 0 & 5Y_{0x} & Y_{0r} \\ Y_{01} & Y_{02} & 0 & 7Y_{0x} & Y_{0r} \\ 0 & 0 & Y_{03} & 9Y_{0x} & Y_{0r} \\ Y_{01} & 0 & Y_{03} & 11Y_{0x} & Y_{0r} \\ 0 & Y_{02} & Y_{03} & 13Y_{0x} & Y_{0r} \\ Y_{01} & Y_{02} & Y_{03} & 15Y_{0x} & Y_{0r} \end{bmatrix} \tag{11}$$

$$\mathbf{V} = [V_c \; V_c \; V_c \; 1 \; V_r]^T \tag{12}$$

TABLE II
THE CONDUCTANCES ON THE EXTENDED CIRCUIT

Parameter	Y_{0x}	Y_{0x}	Y_{01}	Y_{02}	Y_{03}
Solution	Y_{0r}	Y_{0r}	$2\cdot Y_{0r}\cdot V_r/V_c$	$2\cdot Y_{01}$	$4\cdot Y_{01}$

TABLE III
THE CONDUCTANCES OF THE 4-BIT A/D CONVERTER

Parameter	Y_{ix}	Y_{i1}	Y_{i2}	Y_{i3}
Solution for bit 3	Y_{3r}			
Solution for bit 2	Y_{2r}			$2\cdot Y_{2r}\cdot V_r/V_c$
Solution for bit 1	Y_{1r}		$2\cdot Y_{1r}\cdot V_r/V_c$	$2\cdot Y_{12}$
Solution for bit 0	Y_{0r}	$2\cdot Y_{0r}\cdot V_r/V_c$	$2\cdot Y_{01}$	$4\cdot Y_{01}$

and

$$\mathbf{0} = [0\ 0\ 0\ 0\ 0\ 0\ 0\ 0]^T. \tag{13}$$

The conductance values from the solution of (10) will ensure that the transfer function shown as the curve b in Fig. 5 is obtained, ensuring that (3) is satisfied. Therefore, the solution of (10) is also the solution of (3), and the function described by (2) can be performed when the conductances obtained from the solution of (10) are used.

Equation (10) contains 8 equations with 5 unknown parameters. If the solution base of (10) can be formed from five rows in the matrix $\mathbf{Y}$ that are linear-independent, the solution must be that all parameters are zero. It is clear that this solution is not the one we need. To obtain an effective solution, one parameter can be selected as reference parameter, and the solution base can be formed from four rows in the matrix $\mathbf{Y}$ that are linear-independent.

In our solution we select the 1st, 2nd, 3rd, and 5th row to form the base of the solution as they are linear-independent. Equation (10) is then solved with the following equation

$$\begin{bmatrix} 0 & 0 & 0 & Y'_{0x} \\ Y_{01} & 0 & 0 & 3Y'_{0x} \\ 0 & Y_{02} & 0 & 5Y'_{0x} \\ 0 & 0 & Y_{03} & 9Y'_{0x} \end{bmatrix} \cdot \begin{bmatrix} V_c \\ V_c \\ V_c \\ 1 \end{bmatrix} = -Y_{0r}V_r \cdot \begin{bmatrix} 1 \\ 1 \\ 1 \\ 1 \end{bmatrix}. \tag{14}$$

Y_{0r} in (14) is chosen as the reference parameter as the number of parameters exceed the number of equations by 1. The solution is shown in Table II.

Thus with the extended circuit shown in Fig. 2 and the conductances shown in Table II, a 3-bit A/D converter can be extended to a 4-bit A/D converter. The above extending procedure shows, the nature of the 4-bit converter in stability is determined by the 3-bit converter contained. If the 3-bit converter is stable, the 4-bit converter obtained is also stable. This bit extension process forms the basis of the novel design technique for A/D converters based on a hierarchic network proposed.

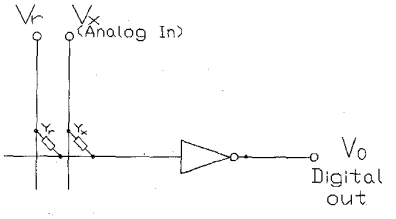

Fig. 6. A 1-bit A/D converter formed by comparator and resistors.

IV. DESIGNING A/D CONVERTERS WITH HIERARCHIC NETWORKS

The analysis above showed that it is easy to extend a 3-bit A/D converter to a 4-bit converter by adding an extra branch circuit, as shown in Fig. 2. Similarly, a 3-bit A/D converter can be achieved by adding a branch circuit to a 2-bit one, and so forth. Using this analogy, a single 1-bit A/D converter can be achieved which will act as the building block for an A/D converter with arbitrary number of bits.

Fig. 6 shows a 1-bit converter formed by a comparator and two resistors. Fig. 7 shows the circuit of a 4-bit A/D converter extended from the 1-bit converter, and its calculated parameter values are shown in Table III. The circuit in Fig. 7 is an asymmetrical network, and it is also a hierarchic network as the output of the lower bit circuits are "governed" by the higher bit circuits.

From Table III, it can be seen that all the conductances, Y_{ix} and Y_{ij}, have a regular order, that is,

$$Y_{i(i+1)} = 2Y_{0r} \cdot V_r/V_C \tag{15}$$

$$Y_{ij} = 2^{j-i-1} \cdot Y_{i(i+1)} \quad (j = i+1, i+2, \ldots, N-1). \tag{16}$$

TABLE IV
THE CONDUCTANCES OF THE 10-BIT A/D CONVERTER

Bit	Y_{ix}	Y_{i1}	Y_{i2}	Y_{i3}	Y_{i4}	Y_{i5}	Y_{i6}	Y_{i7}	Y_{i8}	Y_{i9}
9	Y_{9r}									
8	Y_{8r}									$2\cdot Y_{8r}\cdot P$
7	Y_{7r}								$2\cdot Y_{7r}\cdot P$	$2^1\cdot Y_{78}$
6	Y_{6r}							$2\cdot Y_{6r}\cdot P$	$2^1\cdot Y_{67}$	$2^2\cdot Y_{67}$
5	Y_{5r}						$2\cdot Y_{5r}\cdot P$	$2^1\cdot Y_{56}$	$2^2\cdot Y_{56}$	$2^3\cdot Y_{56}$
4	Y_{4r}					$2\cdot Y_{4r}\cdot P$	$2^1\cdot Y_{45}$	$2^2\cdot Y_{45}$	$2^3\cdot Y_{45}$	$2^4\cdot Y_{45}$
3	Y_{3r}				$2\cdot Y_{3r}\cdot P$	$2^1\cdot Y_{34}$	$2^2\cdot Y_{34}$	$2^3\cdot Y_{34}$	$2^4\cdot Y_{34}$	$2^5\cdot Y_{34}$
2	Y_{2r}			$2\cdot Y_{2r}\cdot P$	$2^1\cdot Y_{23}$	$2^2\cdot Y_{23}$	$2^3\cdot Y_{23}$	$2^4\cdot Y_{23}$	$2^5\cdot Y_{23}$	$2^6\cdot Y_{23}$
1	Y_{1r}		$2\cdot Y_{1r}\cdot P$	$2^1\cdot Y_{12}$	$2^2\cdot Y_{12}$	$2^3\cdot Y_{12}$	$2^4\cdot Y_{12}$	$2^5\cdot Y_{12}$	$2^6\cdot Y_{12}$	$2^7\cdot Y_{12}$
0	Y_{0r}	$2\cdot Y_{0r}\cdot P$	$2^1\cdot Y_{01}$	$2^2\cdot Y_{01}$	$2^3\cdot Y_{01}$	$2^4\cdot Y_{01}$	$2^5\cdot Y_{01}$	$2^6\cdot Y_{01}$	$2^7\cdot Y_{01}$	$2^8\cdot Y_{01}$

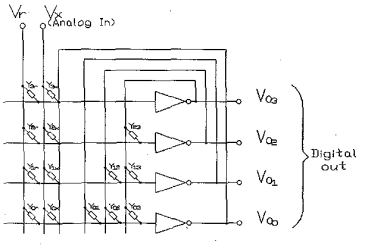

Fig. 7. A 4-bit A/D converter based on the hierarchic network.

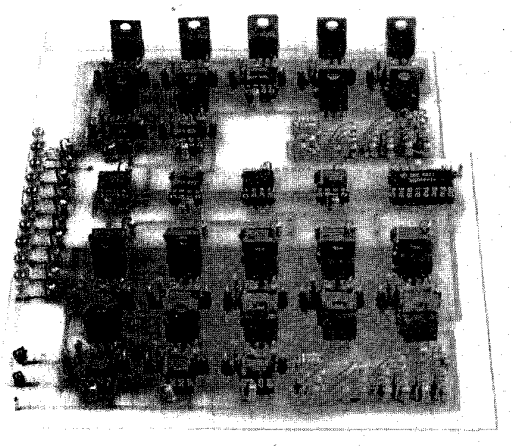

Fig. 8. The prototype of 10-bit A/D converter based on the hierarchic network.

It is thus easy to deduce the conductances with this order in the designs of higher bit number A/D converters. For example, the conductances of a 10-bit A/D converter are deduced and shown in Table IV, with $P = V_r/V_c$.

V. HARDWARE IMPLEMENTATION

Several important details need to be considered in the hardware implementation of the A/D converter. The value of reference voltage, V_r, as well as the value of the resistors connected to the reference voltage, R_{ir}, need to be selected so that the other resistors have practical values. For the optimal operation of the converter, high speed comparators are preferable. As the output of the comparators corresponding to the higher significant bits are required to drive those comparators corresponding to the lower bits, the fan-out ability of the comparator (i.e., the number of comparators that can be driven by a single similar comparator without degradation of its output voltage) should be good. Also the output voltages of the comparators need to be accurate as well as stable to ensure good operation of the A/D converter.

To check the feasibility of the proposed methodology, we built a 5-bit converter and a 10-bit converter which is developed from the 5-bit converter with discrete components, see Fig. 8. In our implementation, the following values were chosen, $V_c = -5$ V, $V_m = 12$ V and $V_r = -5$ V. These voltage values are chosen as they are readily available from power supplies and the voltage regulators commonly used.

VI. ANALYSIS OF NONLINEARITY

The A/D converter proposed is formed by comparators and resistors. Its performance is certainly related to the characteristics of these components. In the following, the nonlinearity of the converter will be analyzed for a clear understanding of the influence of the precision of components and other related values.

An N-bit converter proposed has N comparators. The highest bit is $(N-1)$-bit and lowest bit is 0-bit (see Fig. 8). The input voltage of the ith bit is

$$V_{i\text{net}} = \frac{V_x \cdot Y_{ix} + V_r \cdot Y_{ir} + \sum_{j=i+1}^{N-1} V_{oj} \cdot Y_{ij}}{Y_{ix} + Y_{ir} + \sum_{j=i+1}^{N-1} Y_{ij}}. \quad (17)$$

This equation shows that variations in some resistor values, comparator performance and output voltages of the higher bits, and reference voltage, can affect the value of the input voltage of the ith comparator. From this equation, the differential of V_{inet} can be deduced and its expression is (18) (see (18) at the bottom of the page). Consider the relation shown in (15) and (16), and letting $V_c = V_r$, (18) can be rewritten as (see (19) at the bottom of the page) Equation (19) shows the error sources of V_{inet} can be classified into three parts:

1) the inaccuracy of the reference voltage;
2) the inaccuracy of the resistor values in the ith branch circuit;
3) the error from the higher bits.

The error from the reference voltage can be reduced easily as it is not difficult to build up a high-precision reference voltage source. The influence of the errors from the output voltages of the higher bit comparators is more significant than the inaccuracy in the resistors in the local branch circuit. This can be seen from (19). The equation shows also that the higher the bit number, the stronger the influence of its output voltage. This is actually a characteristic of the hierarchic network structure.

The inaccuracy of the high bit V_{ok} is due to the error of the output voltage of the kth comparator which is related to the electrical characteristic of the comparator and the inaccuracy of the input voltage of this comparator, $V_{k\text{net}}$. They can be reduced by using suitable drive circuits and accurate resistors in the higher bit branch circuits, respectively.

In our prototype of the 5-bit converter, 1% error discrete resistors are used. The integral-nonlinearity and differential-nonlinearity of the converter are shown in Figs. 9 and 10, respectively.

VII. Discussion and Conclusion

A method for designing A/D converters based on a hierarchic network is introduced. In some papers these networks are considered as a type of "neural network," implemented with comparators as neurons and resistors as synaptic weights [1]–[4]. Here, the weights are calculated, but not found by "training" as in most of the other neural networks.

The network introduced in this paper has feedback paths, but, it is a hierarchic asymmetrical network as the outputs of the lower levels (which form the lower bit outputs) are "governed" by the outputs of higher levels (which form the higher bit outputs) and the input signal. When the higher bit outputs are stable, the responses of the lower bits are not dynamic. The A/D converter based on a hierarchic network can be implemented conveniently. However, the resistors used in implementing the A/D converter must be as close as possible to theoretical values. This is because resistors determine the strength of the input signal of the processing element (comparator). It must be pointed out that the errors in resistance values are one source of error in the conversation.

The effects of the output resistance of comparators must be considered in the design. They can be considered as one part of Y_{ij}, unless their values are much smaller than the theoretical value. Therefore, in order to get good accuracy, the performance of the output resistors must be analyzed carefully and the value level of Y_{ij} should also be selected carefully in the design procedure.

The accuracy of the output voltages of the comparators are very important, especially for the higher order bits as they are fed back to the inputs of the lower significant bits and the accumulated error will be presented to the input of the lower significant bits which in turn will produce an inaccurate output.

$$dV_{\text{inet}} = \frac{V_r dY_{ir} + V_x dY_{ix} + \sum_{j=i+1}^{N-1} V_{oj} \cdot dY_{ij}}{Y_{ir} + Y_{ix} + \sum_{j=i+1}^{N-1} Y_{ij}} + \frac{Y_r dV_r + \sum_{j=i+1}^{N-1} Y_{ij} dV_{oj}}{Y_{ir} + Y_{ix} + \sum_{j=i+1}^{N-1} Y_{ij}} - \frac{\left(V_r Y_{ir} + V_x Y_{ix} + \sum_{j=i+1}^{N-1} V_{oj} \cdot Y_{ij}\right)\left(dY_{ir} + dY_{ix} + \sum_{j=i+1}^{N-1} dY_{ij}\right)}{\left(Y_{ir} + Y_{ix} + \sum_{i=j+1}^{N-1} Y_{ij}\right)^2}. \tag{18}$$

$$dV_{\text{inet}} = \frac{V_r dY_{ir} + V_x dY_{ix} + \sum_{j=i+1}^{N-1} V_{oj} \cdot dY_{ij}}{2^{N-i-1} Y_{ir}} + \frac{dV_r + \sum_{j=i+1}^{N-1} 2^{j-i} dV_{oj}}{2^{N-i-1}} - \frac{\left(V_r + V_x + \sum_{j=i+1}^{N-1} 2^{j-i} V_{oj}\right)\left(dY_{ir} + dY_{ix} + \sum_{j=i+1}^{N-1} dY_{ij}\right)}{4^{N-i-1}} \tag{19}$$

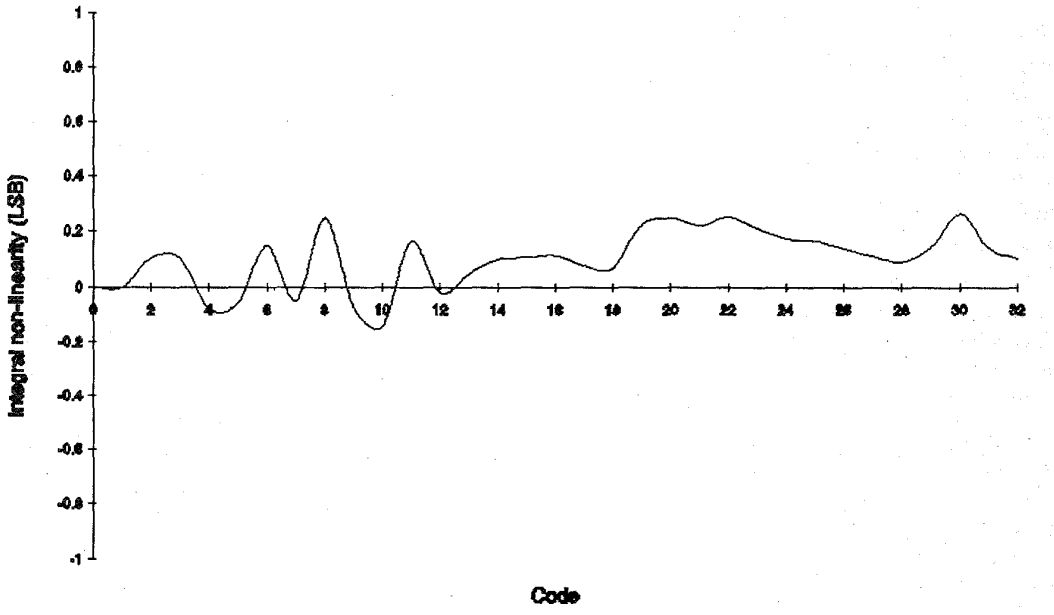

Fig. 9. The integral nonlinearity of the 5-bit A/D converter based on the hierarchic network.

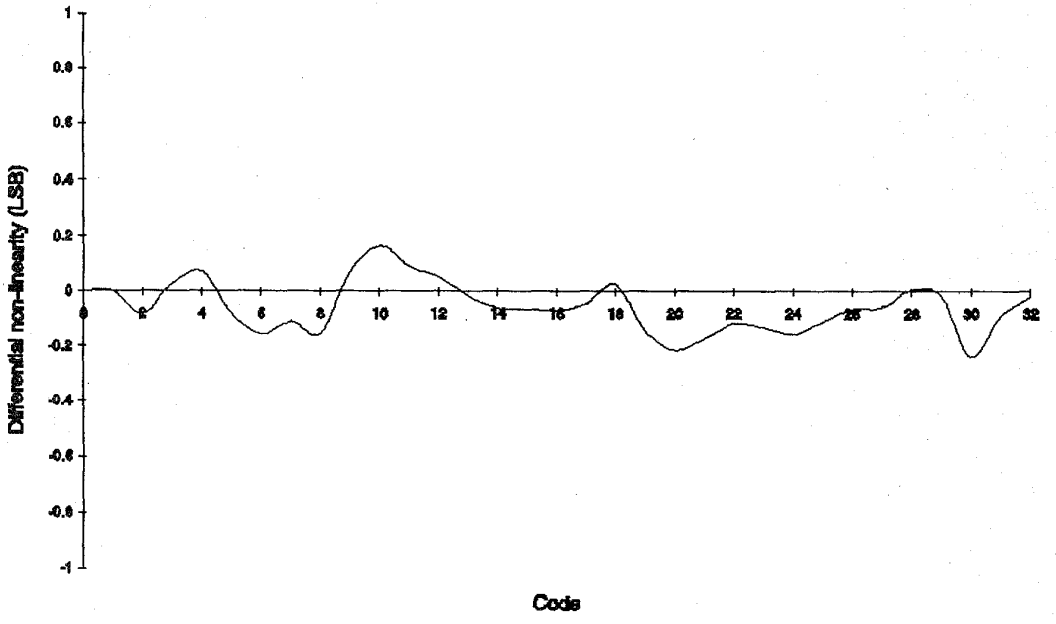

Fig. 10. The differential nonlinearity of the 5-bit A/D converter based on the hierarchic network.

The advantages of the A/D converter introduced in this paper are

1) *Simplicity*: The circuit is extremely simple and therefore is easily fabricated as an integrated circuit chip. It is simpler in comparison with the Hopfield A/D converter. For an N-bit converter, only $1/2 \cdot N \cdot (N+1)$ resistors are needed to form the weights of the network (In the Hopfield converter, the number is $N \cdot (N-1)$).
2) *Speed*: For the N-bit A/D converter, the longest conversion time is almost $N \cdot t_c$, where t_c is the turn over time of comparator. Thus, high-speed A/D converters can be realized.
3) *No clock signals required*: It is troublesome to add a clock timer to A/D converters and to do additional tuning of the clock pulse to suit the requirements of the converter. The A/D converter based on the hierarchic network eliminates the need for a clock signal.
4) *No local minimum points*: The Hopfield network does not always go from an old state to the nearest new stable state. Because of this, the Hopfield A/D converter has to

be reinitialized after every conversion. This requires the use of a high frequency clock signal generator. The new proposed A/D converter dose not have this problem as it does not have any local minimum points. Its output will simply change with respect to the input signal.

REFERENCES

[1] D. W. Tank and J. J. Hopfield, "Simple "neural" optimization networks: An A/D converter, signal decision circuit and a linear programming circuit," *IEEE Trans. Circuits Syst.*, ol. CAS-33, no. 5, pp. 533–541, May 1986.

[2] J. J. Hopfield and D. W. Tank, "Neural computation of decisions optimization problems," *Biological Cybern.*, vol. 52, pp. 141–152, 1985.

[3] P. D. Wasserman, *Neural Computing—Theory and Practice*,New York: Van Nostrand Reinhold, 1988.

[4] O. Barkan, W. S. Smith, and G. Persky, "Design of coupling resistor networks for neural network hardware," *IEEE Trans. Circuits Syst.*, vol. 27, no. 6, pp. 771–779, June 1990.

[5] A. N. Michel and D. L. Gray, "Analysis and synthesis of neural networks with lower block triangular interconnecting structure," *IEEE Trans. Circuits Syst.*, vol. 37, no. 10, pp. 1267–1283, Oct. 1990.

[6] M. P. Kennedy and L. O. Chua, "Circuit theoretic solutions for neural networks—An old approach to a new problem," in *Proc. IEEE Int. Conf. Neural Network*, 1987, pp. II-169–II-176.

[7] B. W. Lee and B. J. Sheu, "An investigation on local minima of Hopfield network for optimization circuits," in *Proc. IEEE Int. Conf. Neural Networks*, 1988, pp. I-45–I-51.

[8] K. V. Keeng, "Hardware implementation of a neural network analog to digital converter," Bachelor Degree thesis, Dept. of Electrical Engineering, National University of Singapore, 1991.

[9] F. Girosi and T. Poggio, "Networks for approximation and learning," in *Proc. IEEE*, Sept. 1990, vol. 78, no. 9, pp. 169–176.

Teck Seng Low (M'83–SM'93) graduated with the B.Sc. degree, first class, and Ph.D. degrees from the University of Southhampton, UK, in 1978 and 1982, respectively.

He joined the National University of Singapore in 1983. He is presently the Director of the Magnetics Technology Centre, a national research center which focuses on magnetic data storage systems. His research interests are in intelligent mechatronics, neural and fuzzy systems, computational electromagnetics, and magnetic recording technology.

Dr. Low's international professional activities include appointment to the Strategic Planning Committee and the Nominations and Appointments Committee of the IEEE and election to the Administrative Committee of the IEEE Industrial Electronics Society. He is currently a member of Singapore's Institute of Standards' electrical products standards committee.

Chao Bi was born in Nanjing, P.R. China. He received the B.Sc. degree in electrical engineering from Hefei Industrial University, China, in 1982, the M.Sc. degree in electrical engineering from Xian Jiaotong University, China, in 1984, and the Ph.D. degree from National University of Singapore in 1995.

His research has included neural networks, signal processing, electric machine theory, electromagnetic field analysis, and optimization technology. He joined th R&D Center, Western Digital (S) Pte Ltd., Singapore, in 1995, where he is presently a senior engineer. His current research interests are micro motor design and control, EMI reduction techniques, and neural networks applications to field analysis.